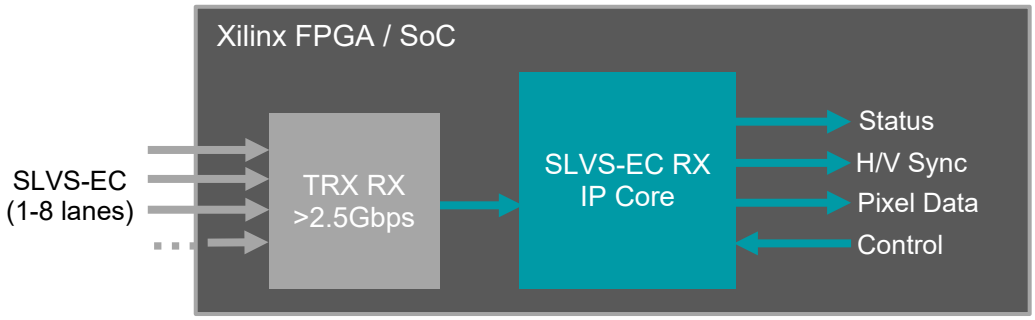
Datasheet

SLVS-EC v2.0 RX IP Core for Xilinx FPGAs & SoCs

The SLVS-EC interface standard has emerged as the high-speed interface for image sensors from Sony. It increases throughput to up to 5 Gbit/s per lane at great signal integrity. Engineers developing solutions using Xilinx FPGAs and SoCs can take advantage of FRAMOS's SLVS-EC RX IP Core, Development Kit, and tested source code examples. Device builders and camera vendors can mitigate design risk while leveraging the benefits of Sony's latest high-speed interface.



Key Benefits & Features:

- Byte-to-pixel conversion for SLVS-EC v1.2 / v2.0
- De-risk integration, reduce time to market
- Reference implementation for evaluation and guidance
- Flexible Lane Support in one IP Core
- Support for all supported RAW bit-depths
- Error correction and ROI overlap support
- AXI4 communication and control

Package

IP Core
- Encrypted RTL
- Source Code Option (VHDL or Verilog)
- Simulation Environment (ModelSim)

Documentation
- User Manual
- Reference Design Example for *EK-U1-KCU105-G*

Verified Xilinx Devices (IP Core)
- Artix-7 (xc7a200tfbg676-2)
- Kintex-7 (xc7k325tffg900-2)
- Zynq-7000 (xc7z045ffg900-2)
- Kintex US (xcku040-ffva1156-2-e)
- Kintex US+ (xcku5p-ffvb676-2-e)
- Zynq US+ (xczu9eg-ffvb1156-2-i-es2)
- Kria™ K26 (xck26)

Product Specification	
Name	SLVS-EC RX IP Core for Xilinx
Type	Receiver (RX)
Input Interface	SLVS-EC V1.2 and V2.0
Output Interface	Pixel Bus
Control Interface	AXI4-Lite
Dynamic Mode Change	Yes (Pixel Format)
Design Environment	Vivado Design Suite 2016.4 and later
Supported Standard and Features	
Compatible Standards	SLVS-EC v1.2, v2.0
Lanes Supported	1, 2, 4, 8 (configurable by user)
Baud Grade(s)	[1]: **1.2 Gbps**, [2]: **2.5 Gbps**, [3]: **5 Gbps**
Pixel Format(s)	8, 10, 12, 14, 16 bits per pixel (RAW) (Dynamic Mode Change)
Embedded Data	Supported
CRC / ECC	Supported (Configurable)
ROI Overlapping	Supported

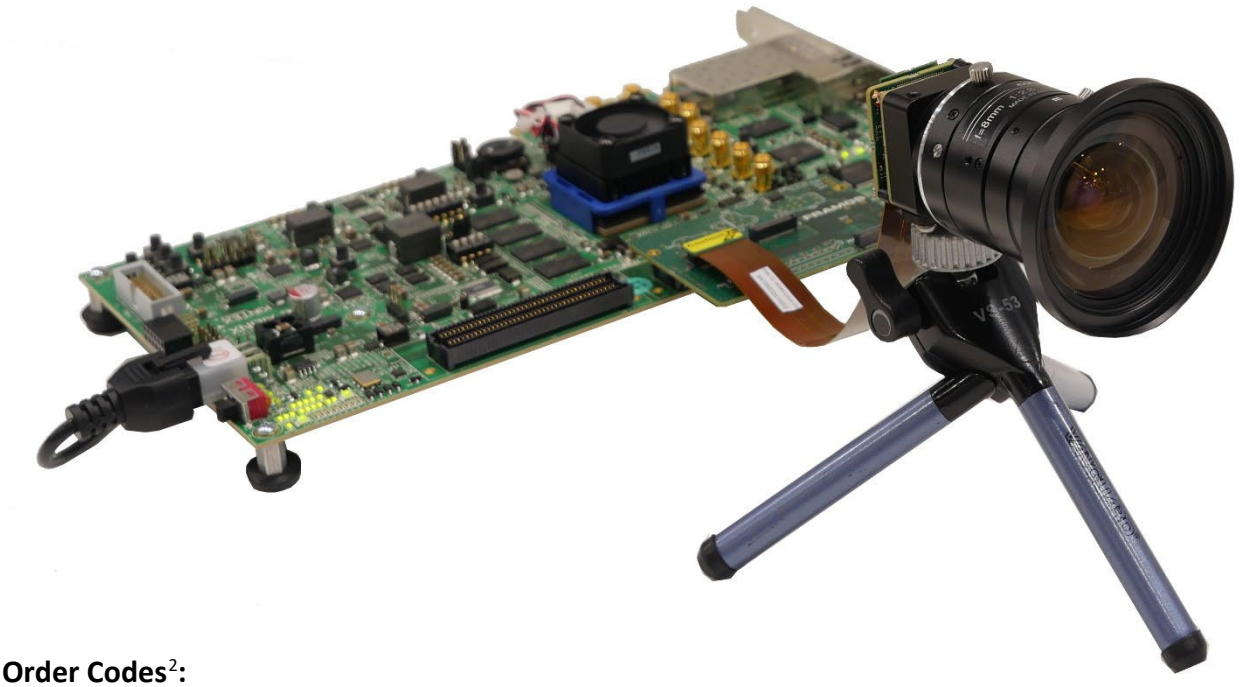
Resource Utilization

The resource utilizations for the various configurations of the IP Core is shown below[1]:

Configuration	1-lane		2-lanes		4-lanes		8-lanes	
Error Handling	**CRC**	**ECC**	**CRC**	**ECC**	**CRC**	**ECC**	**CRC**	**ECC**
Look-up Tables	643	2732	984	3725	1561	6100	3122	10520
Flip-Flops	1181	2467	1538	3059	2279	4174	4045	6575
18k BRAMs	0	0	0	0	0	1	0	2
36k BRAMs	0	5	0	5	0	4	0	5
DSPs	0	3	0	3	0	3	0	3

Development Kit

The SLVS-EC RX IP Core Development Kit from FRAMOS provides you with a ready-to-use hardware environment. It supports your evaluation and demonstrates based on an exemplary and fully documented image pipeline, the integration of the IP Core into a typical camera design.



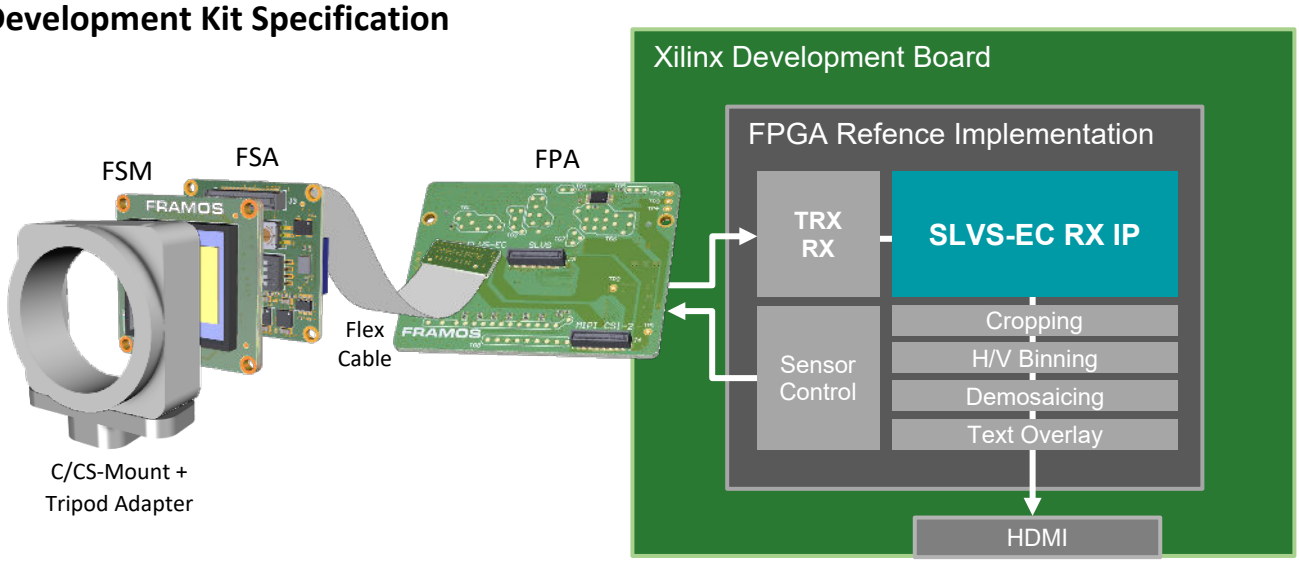
Order Codes[2]:

- FSM-IMX421C/XX1_Devkit-SLVS+EC – *Sony IMX421LQJ, 2.8MP Pregius (Gen 3)*
- FSM-IMX530C/XX1_Devkit-SLVS+EC – *Sony IMX530-AAQJ, 24MP Pregius S (Gen 4)*

[1] Numbers are rounded maximum values and apply to all verified devices.
Source: Utilization reports of Vivado Design Suite 2017.4.

[2] Xilinx Development Board is not included and available from your local Xilinx partner.

Development Kit Specification



Hardware Specification

Package

- FRAMOS Sensor Module (FSM) with C/CS-Mount
- FRAMOS Sensor Adapter (FSA)
- Framos Processor Adapter (FPA)
- Flex Cable 150 mm
- ¼" Tripod Adapter
- Software Download

The Development Kit is a component of the *FRAMOS Sensor Module Ecosystem* and the hardware compatibility exceeds the scope of the IP Core offering. For further information, refer to the appropriate FSM Datasheet.

Hardware Compatibility[3]:

- Artix-7™ (EK-A7-AC701-G)
- Kintex-7™ (EK-K7-KC705-G)
- Zynq-7000™ (EK-Z7-ZC706-G)
- Kintex UltraScale™ (EK-U1-KCU105-G)
- Kintex UltraScale+™ (EK-U1-KCU116-G)
- Zynq UltraScale+™ (EK-U1-ZCU102-G)

Software Specification

Package

- Reference Design Example for EK-U1-KCU105-G[4]
- SLVS-EC RX IP Core for Evaluation (Time Bombed)
- Documentation
  - Reference Design Example description
  - IP Core User Manual

Reference Design Example for Xilinx KCU105-G:

- Supported imagers: FSM-IMX421, FSM-IMX530[4]
- Instantiation SLVS-EC RX IP Core
- Image sensor configuration (Binary)
  - Master mode (free run)
  - 8-Lane SLVS-EC streaming
  - 10 / 12 bit pixel data
  - Full resolution
- Xilinx Transceiver configuration
- Cropping and binning of RAW image stream
- Demosaicing (Bayer to RGB conversion)[5]
- Text overlay (adding statistics)[5]
- 1080p60 output via HDMI (Xilinx Dev. Kit)

Software Compatibility

- Requires Vivado Design Suite 2020.2.

If you have additional questions about this technology, how it would benefit you or want to request project specific image sensor integration support, please direct your request to our FRAMOS imaging experts. We can be reached at: info@framos.com

[3] Supported only in hardware, greyed kits require customers to modify the Vivado Reference Design.
[4] Adjustments to reference design as well as sensor integration and configuration are not part of the IP Core offering.
[5] *Using standard Xilinx LogiCOREs*