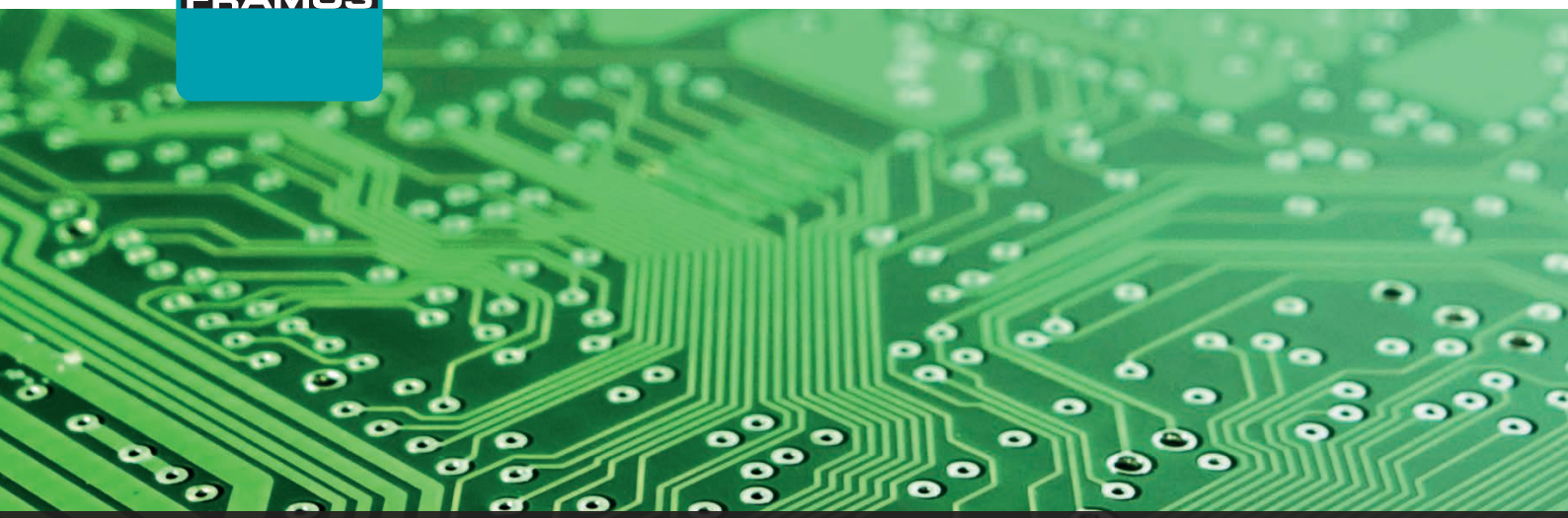
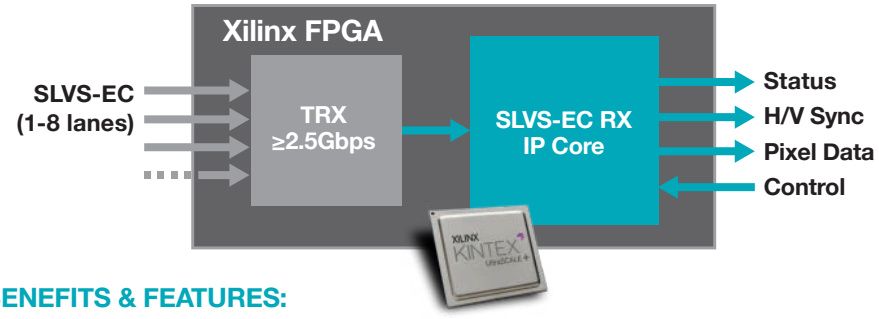


SLVS-EC RX IP Core for Xilinx FPGAs and SoCs

Sony's SLVS-EC interface standard has emerged as the best high speed interface to Sony's best image sensors, enabling higher throughput, greater signal integrity, and simpler designs. Engineers developing solutions using Xilinx FPGAs and SoCs can take advantage of FRAMOS's SLVS-EC RX IP Core, Evaluation Board and tested source code examples. Device builders and camera vendors can de-risk the design while reaping the benefits of Sony's latest high-speed interface.



KEY BENEFITS & FEATURES:

- Byte-to-pixel conversion for SLVS-EC v1.2
- De-risk integration, reduce time to market
- Reference implementation for evaluation and guidance
- Flexible Lane Support in one IP Core
- Support for common RAW bit-depths
- Dynamic mode change support
- AXI4 communication and control

While benefitting from the outstanding sensor performance, SLVS-EC's technological advantages allow significantly simplified designs while extending cable lengths and maintaining signal integrity at high data rates.

The SLVS-EC RX IP Core for Xilinx FPGAs and SoCs provides a trusted, known-good implementation of Sony's preferred interface to advanced image sensors. FRAMOS offers help with the SLVS-EC to keep internal developement teams focused on their core competencies.

SLVS-EC RX IP CORE FOR XILINX FPGAS

The FRAMOS SLVS-EC RX IP Core is a receiver that handles the byte-to-pixel conversion, clock & data recovery, and deserialization of the incoming image data stream. The IP Core provides the customer's FPGA code with a direct pixel bus from the transceivers of the Xilinx FPGA or SoC. Expect versatile support for all SONY sensors that support SLVS-EC version 1.2, at the maximum bit rate, regardless of the number of lanes or bit depth that are required.

CONTENTS

IP Core
Encrypted RTL (VHDL)
Source VHDL
Simulation Environment (ModelSim)

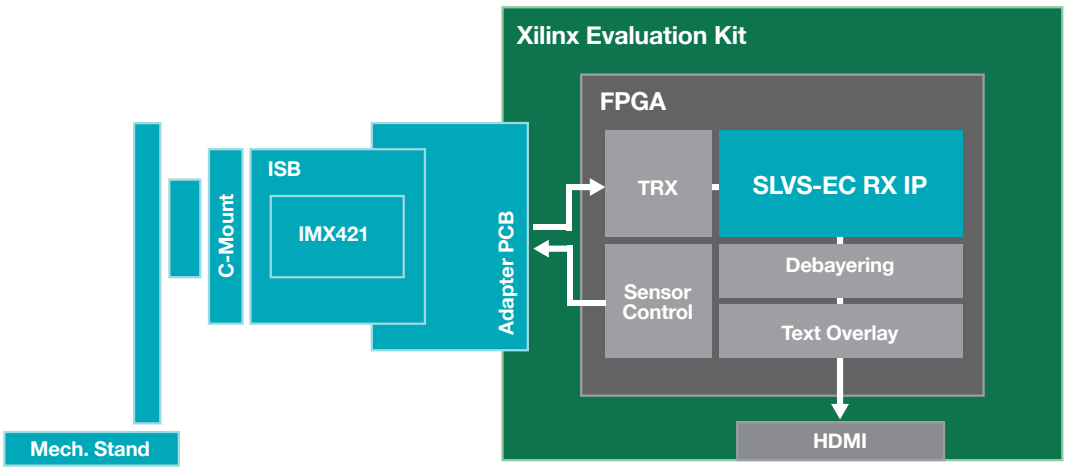
Documentation
User Manual
Reference Implementation (Software)

Supported Device Architectures
Xilinx 7 Series, Ultrascale™, Ultrascale+™

PARAMETER	VALUE
Product Name	SLVS-EC RX IP Core for Xilinx
Standard Version	SLVS-EC v1.2
Type	Receiver (RX)
Control Interface	AXI4
Lanes Supported	1, 2, 4, 8 (configurable by user)
Baud Grade	2
Pixel Formats	8, 10, 12, 14 bits per pixel (RAW)
Dynamic Mode Change	Yes (Pixel Format)
CRC	Yes

EVALUATION BOARD

FRAMOS provides a sensor evaluation extension package for the Xilinx Kintex UltraScale+ FPGA KCU116 Evaluation Kit. The KCU116 kit is available separetely from Xilinx. The extension kit from FRAMOS gives a complete hardware environment for the Sony IMX421 image sensor that incorporates the FRAMOS SLVS-EC RX IP Core. This combination supports evaluation with a fully documented image pipeline.



Hardware

- Image Sensor Board (ISB) with imager
- Adapter to Development Board
- Lens Mount (C-Mount)
- Mechanical Stand

The Xilinx Development Kit is available from your local Xilinx partner.

Software

- SLVS-EC RX IP Core
- Reference Implementation (Software Example)

Documentation

- User Manual
- Assembly instructions
- Software example description

CONTACT

If you have additional questions about this technology or how it would benefit you, our FRAMOS imaging experts are available to answer any questions. We can be reached at: info@framos.com