



USER MANUAL

IMX636 DEVELOPMENT KIT

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Further Documentation and Application Guides

- [FRAMOS IMX636 Devkit Factsheet](#)
- [FRAMOS Sensor Module Ecosystem User Manual](#)
- [FRAMOS Capabilities Collateral](#)
- [FRAMOS Ecosystem Brochure](#)
- [FRAMOS Product Solutions: Event Based Image Sensors](#)
- [FRAMOS Resources Including Training, Whitepapers, Articles](#)
- [FRAMOS News: Sony® Launches The New IMX636](#)
- [PROPHESSEE documentation: Metavision SDK](#)
- [FRAMOS Product Catalog: IMX636AAMR-ES](#)

Navigation and Important Notices

WARNING Warnings appear with information that must be followed to prevent damage to equipment or injury to the end user. Follow these closely. They are indicated by a red prompt and a red border outline.

CAUTION Cautions appear with information that should be followed to protect equipment and to prevent injury to the end user. Follow these closely. They are indicated by a red prompt and a black border outline.

NOTE Notes appear with helpful information and may contain tips, advice, or otherwise useful information to improve your experience.

You may navigate this document quickly when viewing this document electronically with a PDF viewer. In the top header, select the "Section" to return to the section start. Select the "User Manual" to return to the table of contents.

NOTE FRAMOS GmbH has affiliated companies. Affiliates shall mean any corporation, company, or other entity that is in control of, is controlled by, or is under common control with a party hereto, provided that such entity shall be considered a subsidiary only so long such control exists. For purpose of this User Manual affiliates are: FRAMOS Technologies d.o.o., FRAMOS Technologies Inc, FRAMOS Italia, FRAMOS Electronics Ltd, and MAVIS Imaging GmbH (hereinafter all together: FRAMOS)

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Certification and Standards

The equipment described in this document is designed for evaluation and laboratory use, as well as for the integration into electronic devices. The customer is responsible to take all necessary precautions to fulfil regulations and laws of end-customer and target market.

Technical Support

The technical equipment described in this document, be it hardware or software, is delivered as it is and does not include any obligations to FRAMOS to provide technical customer support. Technical support is granted on a per-project basis arbitrary by FRAMOS.

WARNING This kit contains electrostatic-sensitive devices (ESD). Observe ESD handling precautions to avoid damaging the equipment.

Handling ESD Sensitive Components

The electronic components like Printed Circuit Boards (PCB) described in this document are sensitive to Electrostatic Discharge (ESD) and need to be handled with high care in static controlled environments. It is strongly recommended to follow the general handling practices for ESD sensitive parts, that include, but are not limited to, the following points:

- Treat all PCBs and components as ESD sensitive
- Assume that you will damage the PCB or component if you are not ESD conscious
- Handling areas must be equipped with a grounded table, floor mats and wrist strap
- A relative humidity level must be maintained between 20% and 80% non-condensing
- PCBs should not be removed from their protective package, except in a static controlled location
- PCBs must be handled only after personnel have grounded themselves via wrist straps and mats
- PCBs or components should never come in contact with clothing
- Try to handle all PCBs only by their edges, preventing contact with any components

FRAMOS is not responsible for ESD damage caused by misuse.

Life Support Applications

These products are not designed for use in life support systems, appliances, or devices where malfunction of the products can reasonably be expected to result in personal injury. Customers, Integrators and End Users using or selling these products for use in such applications do so at their own risk and agree to fully indemnify FRAMOS for any damages resulting from any improper use or sale.

CE-Declaration

This equipment is in compliance with the essential requirements and other relevant provisions of the following RoHS Directives: Directive 2011/65/EU and (EU) 2015/863.



RoHS

The RoHS Directive (Restriction of Hazardous Substances) complements the WEEE Directive by severely restricting the presence of specific toxic substances in electronic equipment at the design phase, thereby reducing the environmental impact of discarding such products at the end of their useful life. FRAMOS Technologies d.o.o. is committed to complying with this Directive and has worked in collaboration with its suppliers to evaluate the new restrictions, to identify relevant exemptions, and to substitute environmentally benign, compliant alternative materials in its product components and manufacturing processes. Subject to the available exemptions, FRAMOS Technologies d.o.o. products were compliant with the RoHS Directive for its products.



Materials declarations comply with EN 63000:2018 requirements for RoHS Technical Documentation. EU Declaration of conformity according to RoHS are issued on customer demand.

REACH

FRAMOS neither manufactures nor imports chemical substances.

FRAMOS is well aware of:

- The requirements of REACH regulation of the European Council (EC) No. 1907/2006
- The SVHC Candidate List
- Our obligations concerning safety datasheets as well as informing customers



WEEE

The WEEE Directive obliges manufacturers, importers, and/or distributors of electronic equipment to label the equipment for recycling and to provide for recycling of the electronic equipment at the end of its useful life. FRAMOS is committed to complying with the WEEE Directive (as implemented in each EU member state). In accordance with the requirements of the Directive, FRAMOS Technologies d.o.o. has labelled its electronic products that are shipped. The WEEE label and instructions for disposal are as follows:

Instructions for Disposal of Waste Equipment by Users in the European Union

This symbol on the product or its packaging indicates that this product must not be disposed of with other waste. Instead, it is your responsibility to dispose of your waste equipment by handing it over to a designated collection point for the recycling of electrical waste and electronic equipment. The separate collection and recycling of your waste equipment at the time of disposal will help conserve natural resources and ensure that it is recycled in a manner that protects human health and the environment. For more information about where you can drop off your consumer waste equipment for recycling, please contact your local city recycling office or the dealer from whom you originally purchased the product.

Electro Magnetic Compliance (EMC)

The FRAMOS Sensor Module Ecosystem are OEM components/devices and are provided at the open board level. Electrical components with open design do not comply with standards for electromagnetic compatibility as the unshielded circuitry enables electromagnetic interference with other electronic devices.



INTRODUCTION

This chapter briefly describes FRAMOS products, support, and service offerings that may be of special interest to you as you take your product to market.

About FRAMOS

FRAMOS is an imaging expert, trusted advisor, and vision solutions provider. Since 1981, FRAMOS implements the best current and emerging imaging technologies to address specific customer requirements and applications. FRAMOS meets these requirements with advanced and proven imaging components from a global network of renowned partners and with FRAMOS IP.

More than 180 FRAMOS employees world-wide are passionate about the unlimited potential of imaging and help customers achieve the optimum results from every possible scenario.

FRAMOS drives and ensures the entire product development journey from POC, through prototyping, to mass production. FRAMOS carefully selects imaging components, like image sensors, lenses, or various 3D technologies, and offers custom developments tailored to individual needs and time frames.

FRAMOS listens and understands customer challenges. With innovative solutions FRAMOS ensures successful project outcomes and develops long-term customer relations. For more information visit: www.amos.com, [LinkedIn](#) or [Twitter](#).

FRAMOS Sensor Module Ecosystem

The FRAMOS Sensor Module (FSM) Ecosystem consists of FRAMOS Sensor Modules, Adapters, Software, and Sources. It provides one coherent solution supporting the whole process of integrating image sensors into embedded vision products.

Within the development phase, electrical design references and driver sources provide guidance with a solid and proven baseline to quickly port into individual system designs, decreasing risk and efforts.

Reference implementations and sample applications deliver images immediately after installation with V4L2 support, and provide comfortable integration at full control.

Off-The-Shelf Hardware:

- FRAMOS Sensor Modules from stock, ready for evaluation and prototyping.
- Versatile adapter framework, allowing flexible testing of different modules on different processing boards.
- FRAMOS Sensor Adapter: Connect one or multiple FSM + FSA to a specific processor board.
- Supporting a variety of single board computers and processor boards like the NVIDIA Jetson™ Family.
- Linux V4L2 drivers with basic sensor node control.
- FRAMOS SLVS-EC IP Core Reference Implementation.

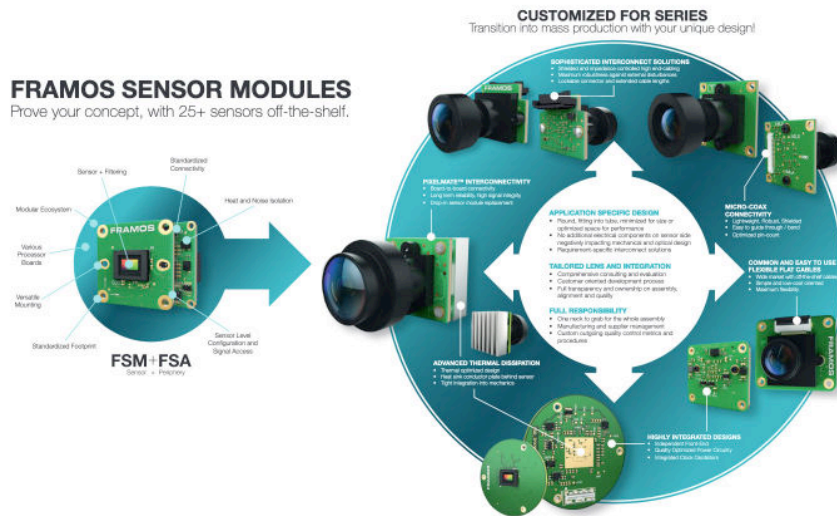
Kickstart Software Package for NVIDIA™

To further the off-the-shelf solutions, the Ecosystem supports you on a per-project basis with:

- Driver sources allowing the focus on application specific scope and sensor features
- Electrical references for FSA and FPA, supporting quick and optimized embedding of FSMs
- Engineering services via FRAMOS and its partners, allowing you to focus on your product's unique value

"From lenses, mechanicals and cables— all needed imaging accessories from one source."

Materials and Services



Hardware

- FRAMOS Sensor Module Development Kits

Individual Parts:

- FRAMOS Sensor Modules (FSM) - Sensors on PCB, with filtering and versatile connector
- FRAMOS Sensor Adapters (FSA) - Sensor periphery and PixelMate™ interface, optional data conversion
- FRAMOS Functional Adapters (FFA) – Sensor independent data and interface adaption, pre-processing
- FRAMOS Processor Adapters (FPA) – Specific for various processor / development boards
- FRAMOS Module Accessories – Cables, mounts, mechanical adapters, etc.

Design Sources

- Software Driver Sources
- Electrical References for FSA, FFA and FPA (Schematics)

Design Services

- Off-the-shelf hardware customization including size, shape, connector and extended functionality
- Software customization and extension
- Processor board integration support
- Sensor and features support, image pre-processing

Software

- Driver and software examples for devices of the NVIDIA Jetson™ family
- FPGA reference implementations for SLVS-EC based image sensors

- Sensor characterization and ISP tuning
- Tailored production and quality assurance processes
- Optimization for volume production
- Lens assembly and alignment
- Standard conformity and certification



PRODUCT DESCRIPTION

The following chapter describes the contents of the FSM-IMX636 Development Kit contents and lists the components to ensure you have everything you need.

Overview

The FSM-IMX636 Devkit delivers high resolution, speed, and temporal resolution with “Event Based Sensing” technology in a compact package for embedded systems engineers. This Devkit integrates the IMX636-AAMR-C Event-based Vision Sensor released by Sony Semiconductor Solutions, and realized in collaboration between Sony and PROPHESSEE. This Devkit comes complete with; a sensor board with lens, all needed adapters, accessories and drivers. Prototype quickly and capture ultra-fast moving objects, or even vibration frequencies of machine components - at a fragment of the data rate, processing efforts, and power consumption of conventional frame based image sensing.

Where conventional image processing algorithms are not applicable, the support of the PROPHESSEE Metavision® Intelligence Suite closes the gap. It provides customers with a proven vision toolkit containing computer vision and machine learning supported modules for event data processing, analytics and visualization.

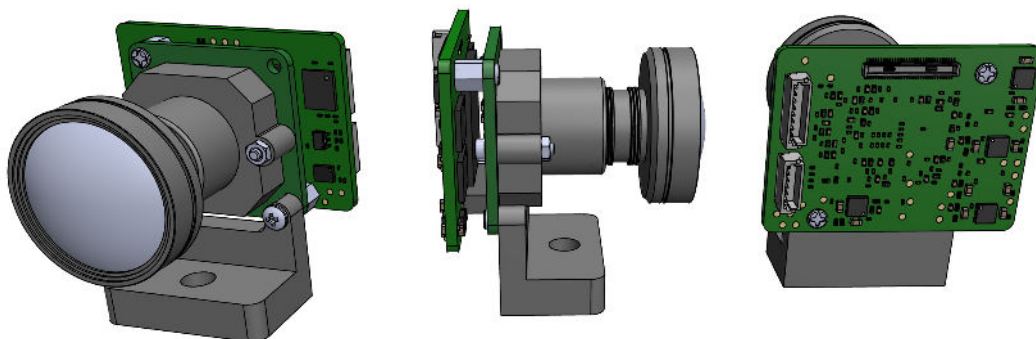


Figure 1. Model view of the front-end assembly in three profiles - callouts on following pages.

Order Code:

FSM-IMX636E/TXA_Devkit-Single-V1A

Item	Description	Qty
FSM-IMX636E-000-V1A	FRAMOS Sensor Module with Sony® IMX636	1
FPL-10006624, M12-Mount	Lens mount assembled with passive alignment	1
FPL-300588, M12-Lens	Optic lens (screwed in, not focused, not glued)	1
FSA-FT27/A-001-V1A	FRAMOS Sensor Adapter with Crosslink NX FPGA	1
FMA-MNT-TRP1/4-V1C	Tripod Adapter with screws (attached)	1
FMA-FC-150/60-V1A	Flex Cable, PixelMate™ (CSI-2), 150 mm	1
FMA-CBL-FL-150/8-V1A	Cable (included for flashing)	1
FPA-4.A/TXA-V1B	FRAMOS Processor Adapter	1
Quick Start Guide	Printed in box with instructions and disclaimers	1

NOTE The NVIDIA processor board for Jetson AGX Xavier™ and AGX Orin™ is supported.



GETTING STARTED

The following chapter describes the hardware assembly procedures according to the FSM-IMX636 Development Kit.

Tools

None.

Supplies

Additional supplies may be required and are not included in this kit:

- NVIDIA® Jetson Xavier™ AGX or AGX Orin™ developer kit
- Display monitor for configuration and operation
- HDMI cable for display monitor connection
- USB hub (2.0 or 3.0 port options) to connect input/output peripherals to the processor board
- USB type-C to USB A (3.0) cable for processor board flashing
- Optional: ethernet cable (RJ45) for remote development

WARNING Never connect an FSM directly (without FSA) to an FPA, or a carrier that was not designed explicitly for this purpose.

The FSM Ecosystem consists of a large set of components using standardized connectors. The compatibility among these components is not ensured by the connector itself – mixing components that are not compatible may lead to permanent damage.

WARNING Do not assemble equipment while the device is powered on. Disconnect power supplies before assembling equipment. Power on the devices per the manufacturer's startup procedures.

Step 1: Unpack the FRAMOS Development Kit.

Unpack the FSM-IMX636 Devkit contents. Inspect the front-end assembly referencing the illustration below.

CAUTION If any visual damage or deviation from the illustrations below are found, approach your FRAMOS contact and do not operate the equipment.



Figure 2. Front views of the IMX636 front-end assembly.

NOTE The front-end assembly may ship with the PixelMate™ (FMA-FC-150/60-V1A) connected. Verify the connection is secure and pin 1 to pin 1 is aligned as indicated in the following pages.

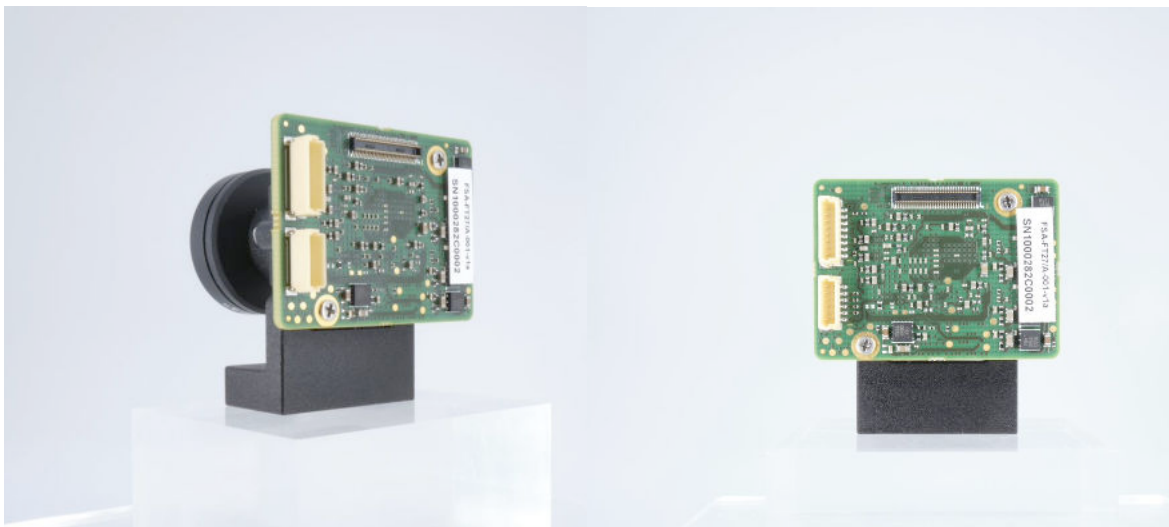


Figure 3. Rear views of the IMX636 front end assembly.

Step 2: Connect the PixelMate™ to the Front End.

Connect the PixelMate™ cable (FMA-FC-150/60-V1A) to the pre-assembled front-end by carefully aligning pin 1 to pin 1 as marked.

WARNING Connect by mating pin 1 to pin 1 as illustrated. Do not invert the pinout orientation during installation. Failure to orient the cable connection as illustrated will lead to permanent equipment damage.

NOTE This step is only required if the front-end did not ship with the PixelMate™ (FMA-FC-150/60-V1A) connected.



Figure 4. Example view of the pin 1 to pin 1 connection.

Step 3: Connect the FPA to the Processor Board.

Connect the FPA (FPA-4.A/TXA-V1B) to the processor board.

NOTE If configuring up a multiple camera setup, reference the FPA appendix pages to ensure the DIP switch SW1 settings are correct according to your setup.

NOTE For single camera use, all DIP switch SW1 settings can be left as "OFF". For your convenience, this product ships with the DIP switch SW1 settings to "OFF".

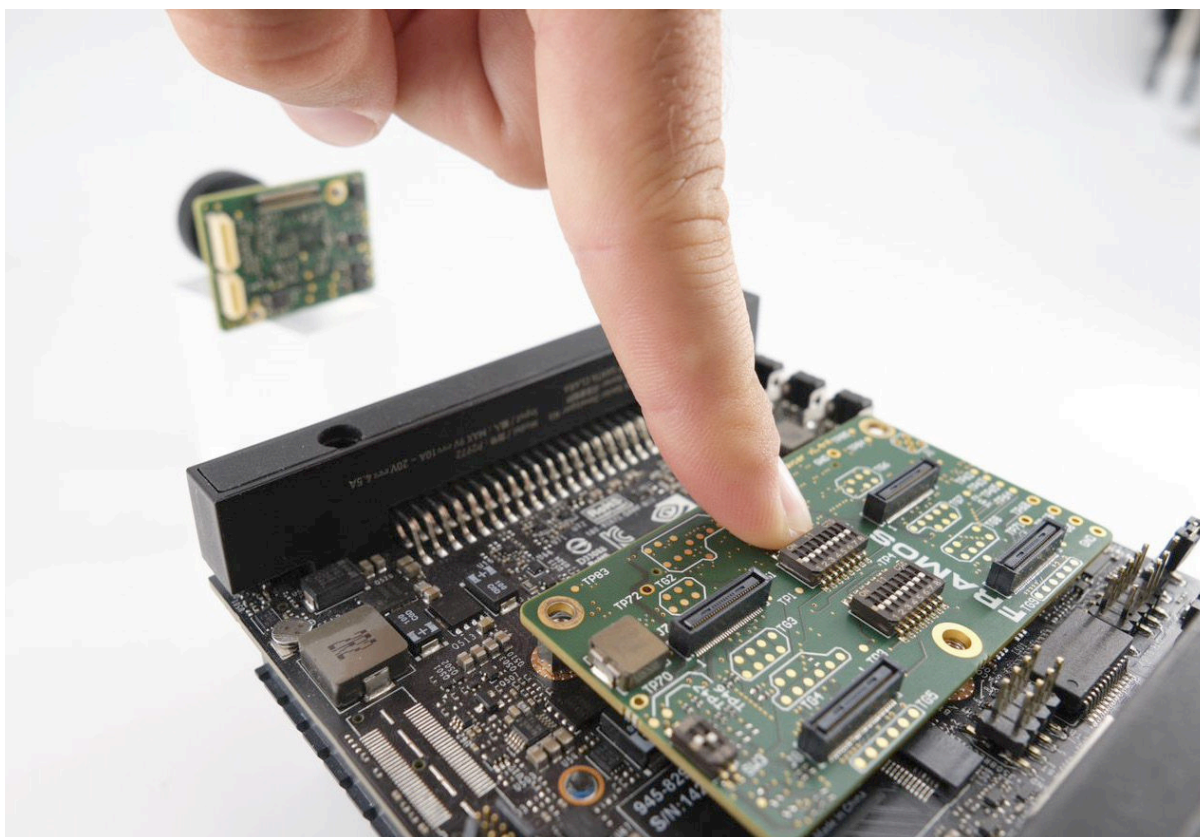


Figure 5. Example view of the FPA to processor board connection.

Step 4: Connect the PixelMate™ to the FPA.

Connect the other side of the PixelMate™ (FMA-FC-150/60-V1A) cable to the FPA (FPA-4.A/TXA-V1B) by aligning pin 1 to pin 1 as marked.

WARNING Connect by mating pin 1 to pin 1 as illustrated. Do not invert the pinout orientation during installation. Failure to orient the cable connection as illustrated will lead to permanent equipment damage.

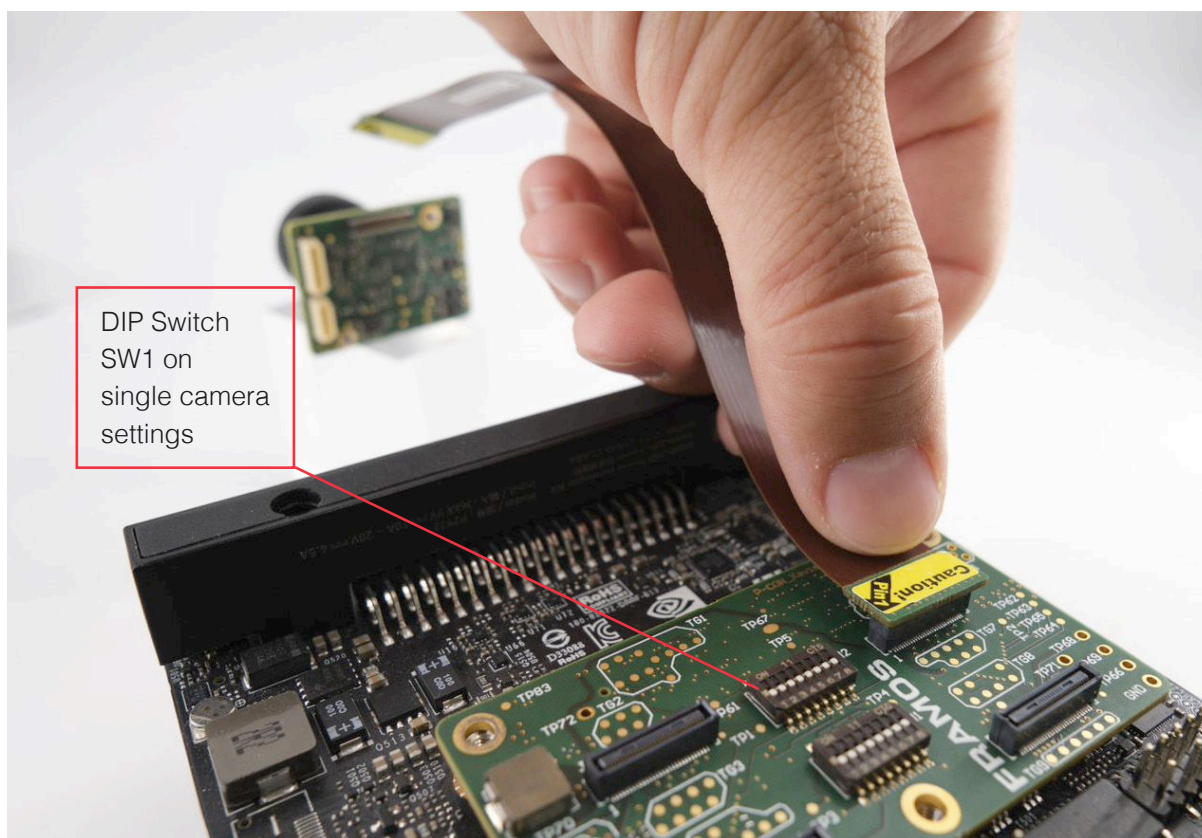


Figure 6. Example view of the pin 1 to pin 1 connection.

NOTE The above illustration depicts a single camera setup. Note the difference in DIP switch SW1 settings when compared against a multiple camera setup per the data in the FPA appendix pages.

Step 5: Prepare the Processor Board.

Prepare the processor board by completing the following:

Substep 1. Connect the unpowered processor board to the required peripheral devices including:

- Item 1 - **Display:** Connect an HDMI cable for display monitor connection
- Item 2 - **USB Peripherals:** Connect the HUB for input/output peripherals (keyboard, mouse) to the processor board via the USB (2.0 or 3.0) port
- Item 3 - **Network:** (Optional) Using an RJ45 ethernet cable for remote development and updates
- Item 4 - **Flashing:** Connect the USB type-C to USB A (2.0 or 3.0) cable for processor board flashing according to the instructions of the processor board manufacturer

Substep 2. Connect the power supply specified by the manufacturer of your processor board.

Substep 3. Follow the startup instructions of the processor board to power on.

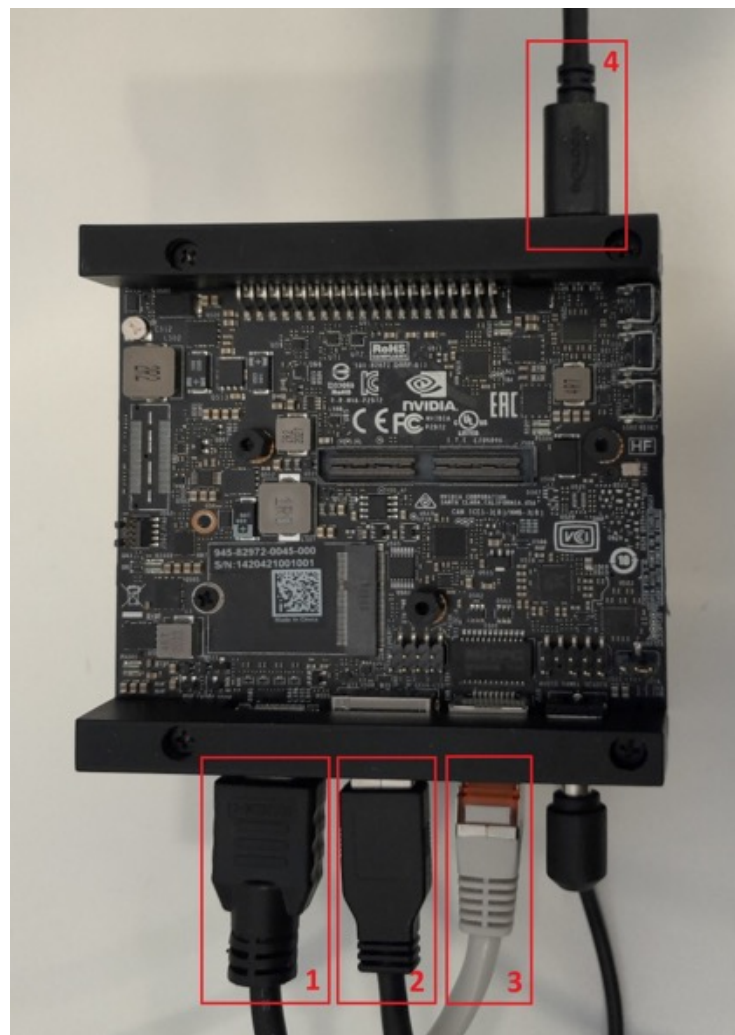


Figure 7. Example view with callouts of the processor board setup.

Step 6: Proceed to Driver and Software Installation.

Proceed with the Driver and Software Installation instructions described in the following chapter.



Figure 8. Completed assembly of the FSM-IMX636 Devkit.



DRIVER AND SOFTWARE

The following chapter provides detailed instruction on how to install the required drivers and software once the hardware is assembled.

Tools

None.

Supplies

Additional supplies may be required and are not included in this kit:

- User Guide – “NVIDIA Jetson Family” (the latest version, FSM_Jetson_UserGuide_vx.x.x.pdf)

Software package including:

- Sensor Driver (for the latest supported JetPack version, framos-imx636-driver-x.x.x.x_arm64.deb)
- Common Driver (for the latest supported JetPack version, framos-common-driver_x.x.x.x_arm64.deb)
- FRAMOS plugin for Metavision® Software (for the latest supported version, framos-imx636-plugin_x.x.x.x_arm64.deb)
- Optional: Metavision® Software User Guide (the latest version, FSM_OpenEB_Software_UserGuide_vx.x.x.x.pdf) to provide supporting information as applicable to your specific use case

NOTE Latest revisions are indicated in this procedure by placeholders ‘x.x.x.x’ or ‘vx.x.x’. Select the latest released driver or guide at the time of download unless otherwise specified.

NOTE Complete all steps in ‘Getting Started’ before beginning the below steps. The starting state requires that the processor board and the FSM-IMX636 Development Kit are powered on and connected.

Step 1: Download the Required Drivers and Guides.

Visit our product documentation page at www.framos.com/fsm-startup to download the following documents:

- User Guide – “NVIDIA® Jetson Family” (the latest version, FSM_Jetson_UserGuide_vx.x.x.pdf)

Software package including:

- Sensor Driver (for the latest supported JetPack version, framos-imx636-driver-x.x.x.x_arm64.deb)
- Metavision® Software (for the latest supported version, framos-imx636-plugin_x.x.x.x_arm64.deb)
- Common Driver (for latest supported JetPack version, framos-common-driver_x.x.x.x_arm64.deb)

NOTE Latest revisions are indicated in this procedure by placeholders ‘x.x.x.x’ or ‘vx.x.x’. Select the latest released driver or guide at the time of download unless otherwise specified.

Step 2: Perform the Software Installation Process.

Follow the software installation steps provided in the OpenEB Software User Guide (the latest version, FSM_OpenEB_Software_UserGuide_vx.x.x.x.pdf).

Step 3: For Advanced Case Use:

Such as horizontal or vertical Crosslink-NX blanking, see the Software section of the appendix pages to extend the basic software installation instructions accordingly.



APPENDIX

The following chapter provides additional supporting information on the individual components of the FSM-IMX636 Development Kit.

NOTE This page is intentionally left blank.

System Block Diagram

The following diagram is a system overview of the FSM-IMX636 Devkit front-end assembly. Reference the individual segments as they appear in the following topics for better readability. From left to right, the FSM, FSA and FPA / Processor Board can be viewed quickly by clicking the link when this document is being read electronically.

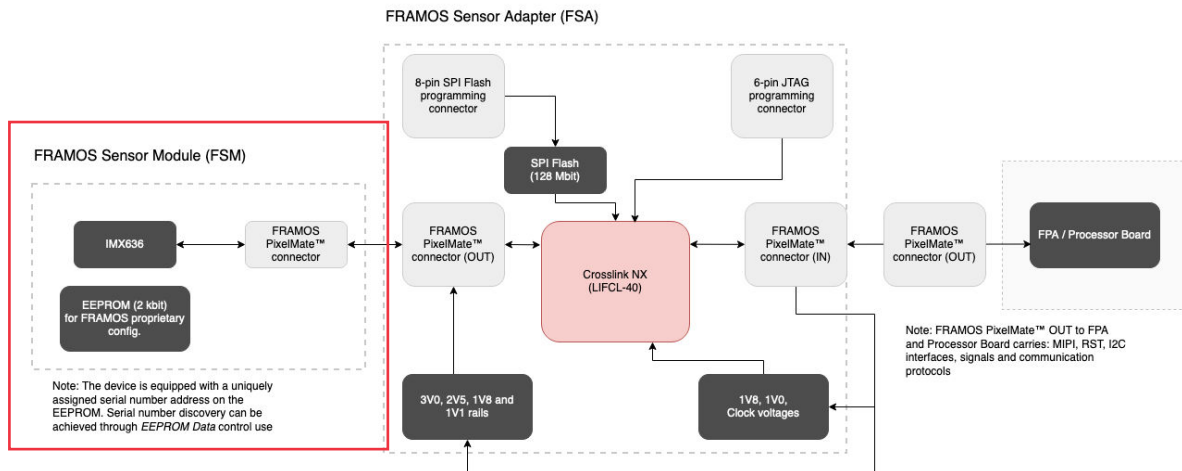
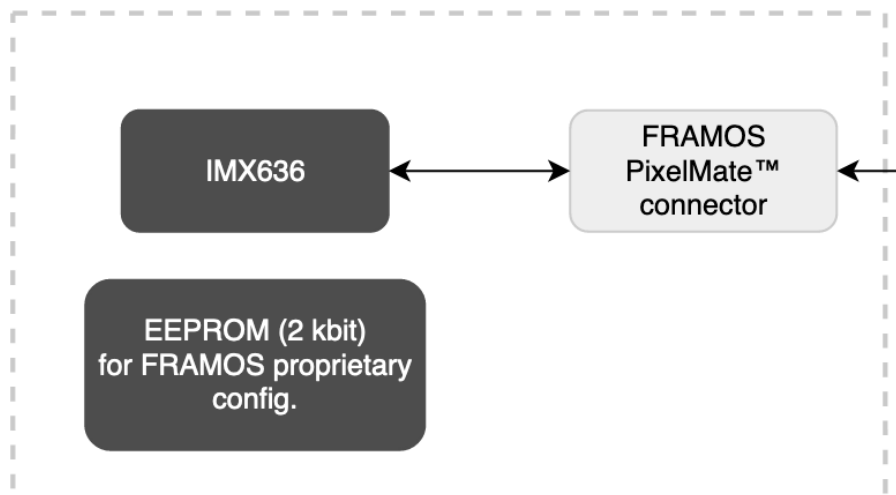


Figure 9. System block diagram.

System Block Diagram 1: FRAMOS Sensor Module with FSM-IMX636 (EVS)

[FRAMOS Sensor Module](#) segment will be covered in the FSM appendix pages and includes the EVS image sensor, EEPROM, and EVT data blanking details.

FRAMOS Sensor Module (FSM)



Note: The device is equipped with a uniquely assigned serial number address on the EEPROM. Serial number discovery can be achieved through *EEPROM Data* control use

Figure 10. FSM view of the System Block Diagram.

System Block Diagram

The following diagram is a system overview of the FSM-IMX636 Devkit front-end assembly. Reference the individual segments as they appear in the following topics for better readability. From left to right, the FSM, FSA and FPA / Processor Board can be viewed quickly by clicking the link when this document is being read electronically.

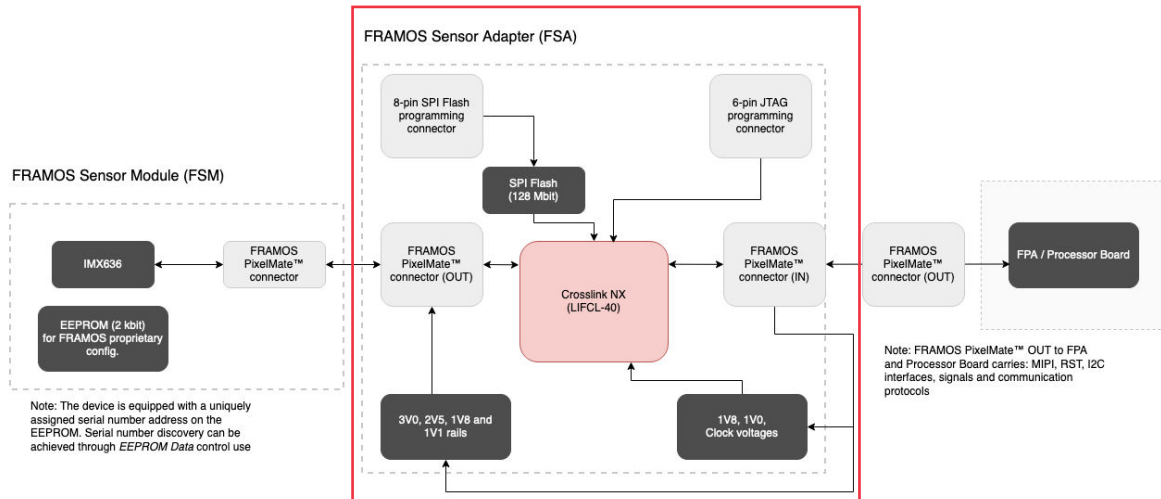


Figure 9. System block diagram.

System Block Diagram 1: FRAMOS Sensor Adapter with Crosslink NX (FPGA)

The [Crosslink NX](#) segment will be covered in the FSA appendix pages and includes the firmware details, power, clocking, and MIPI variable-to-fixed frame conversion.

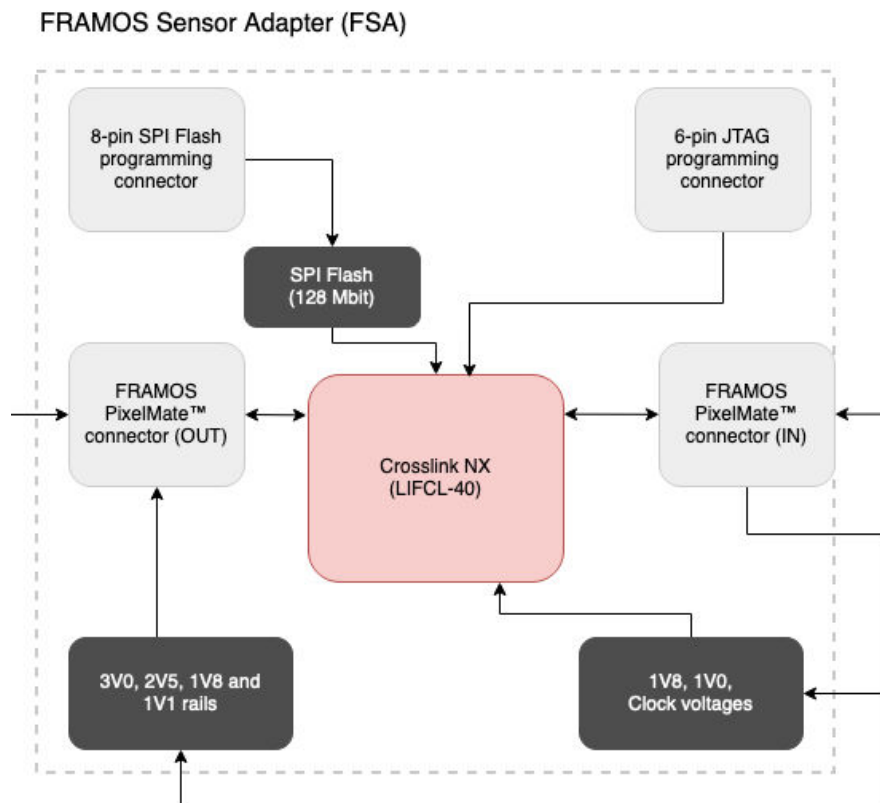


Figure 11. FSA view of the System Block Diagram.

System Block Diagram

The following diagram is a system overview of the FSM-IMX636 Devkit front-end assembly. Reference the individual segments as they appear in the following topics for better readability. From left to right, the FSM, FSA and FPA / Processor Board can be viewed quickly by clicking the link when this document is being read electronically.

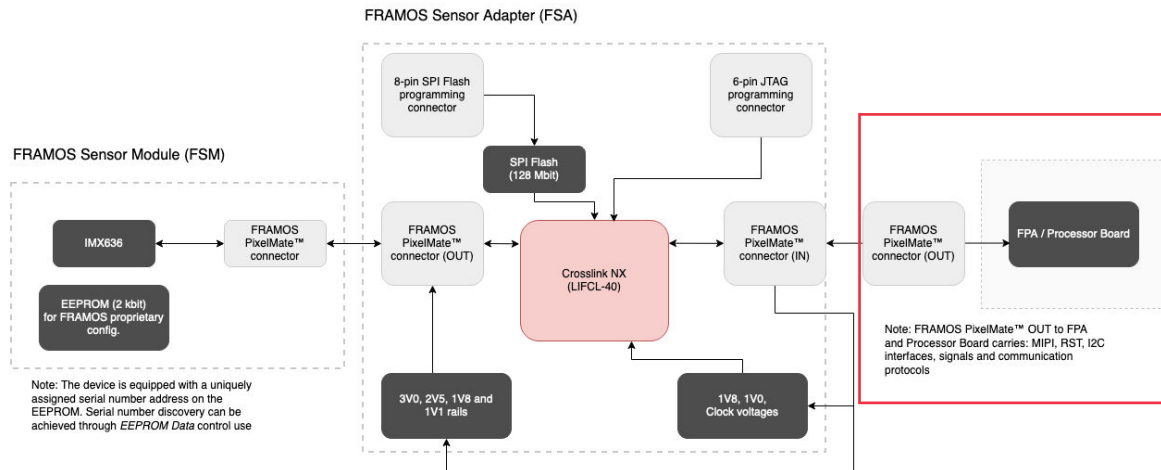
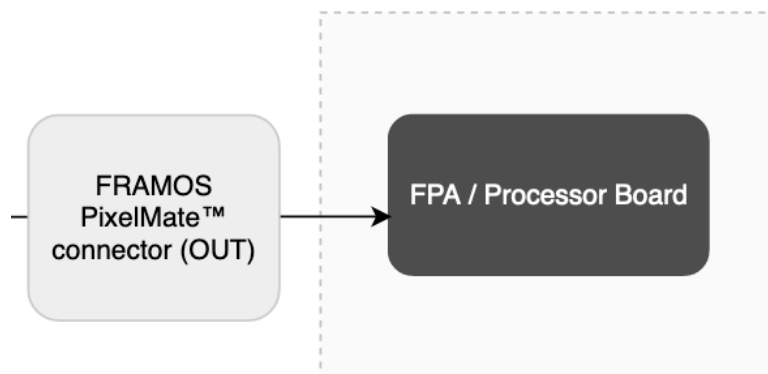


Figure 9. System block diagram.

System Block Diagram 1: FRAMOS Processor Adapter, MIPI, RST, I2C comms.

The [FRAMOS Processor Adapter \(FPA\)](#) segment will be covered in the FPA appendix pages and includes the multi-camera synchronization details.



Note: FRAMOS PixelMate™ OUT to FPA and Processor Board carries: MIPI, RST, I2C interfaces, signals and communication protocols

Figure 12. FPA view of the System Block Diagram.

FRAMOS Sensor Module (FSM)

The FRAMOS Sensor Module (FSM) incorporates the IMX636-AAMR-C image sensor and an Electrically Erasable Programmable Read-Only Memory (EEPROM) that stores a unique serial number for camera identification. Additionally, the EEPROM can accommodate an extra 2 Kb Inter-Integrated Circuit (I2C) configuration if required.

The image sensor supports SLAMODE, EXTTRIG, and SYNC (XVS). Additionally, the image sensor follows the MIPI standard and utilizes 2 MIPI lanes, which can transfer data at a maximum rate of 1.5 Gbps per lane. The FRAMOS Sensor Module is connected to the FRAMOS Sensor Adapter through a standard 60-pin PixelMate™ connector, and it is shipped pre-connected to the FSA at J1 (as indicated below).

For more information on the regular operation of the FSM, please refer to the FRAMOS Sensor Module Ecosystem User Manual. The following information pertains to the IMX636 Development Kit.

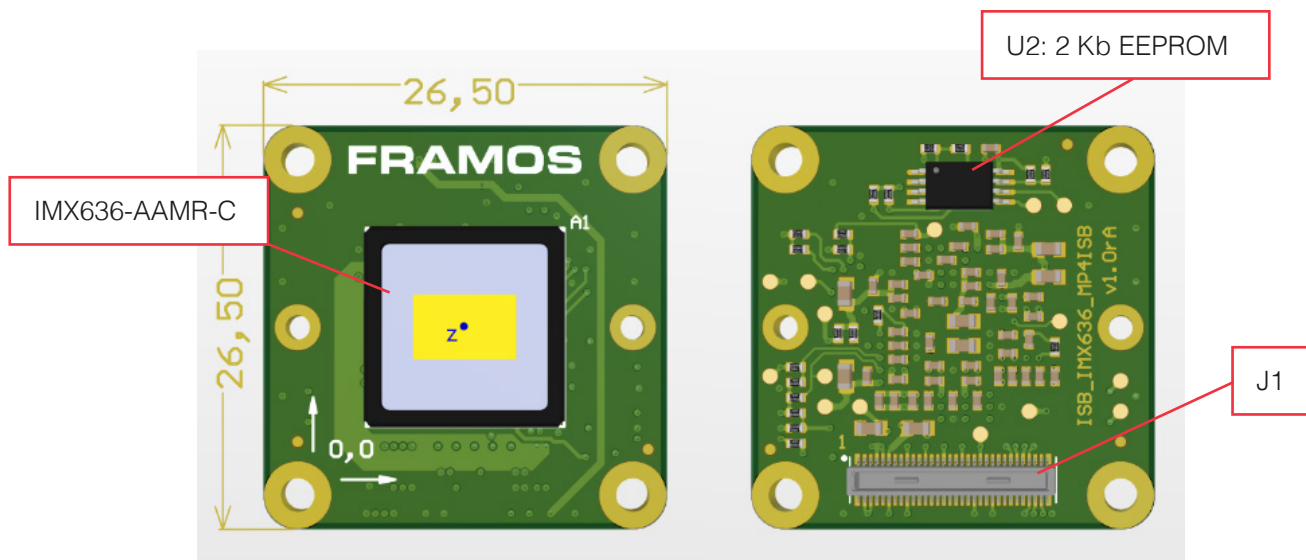


Figure 13. Model view: Framos Sensor Module (FSM) of the FSM-IMX636 Devkit.

NOTE U2: an EEPROM with an additional 2 Kb I2C storage capacity, and a unique serial number to identify the EVS sensor module.

NOTE J2: 60 pin interconnect interfacing with the FSA. Data is routed from here to the FSA for event signal processing.

FRAMOS Sensor Module (FSM) Blanking

The Sony IMX636 event-based vision sensor (EVS) is an image sensor that captures changes in light intensity for each pixel separately. It transmits MIPI CSI-2 frames with a variable line length, depending on the scene movements. Information is only transmitted when there is a change in light intensity. **As a result, the frame can have a variable number of lines, which requires conversion to a fixed size frame.**

The image sensor is configured to transmit over two MIPI lanes, each with a speed of 1500 Mbps.

An example of the image sensor transmission is shown in the images below:

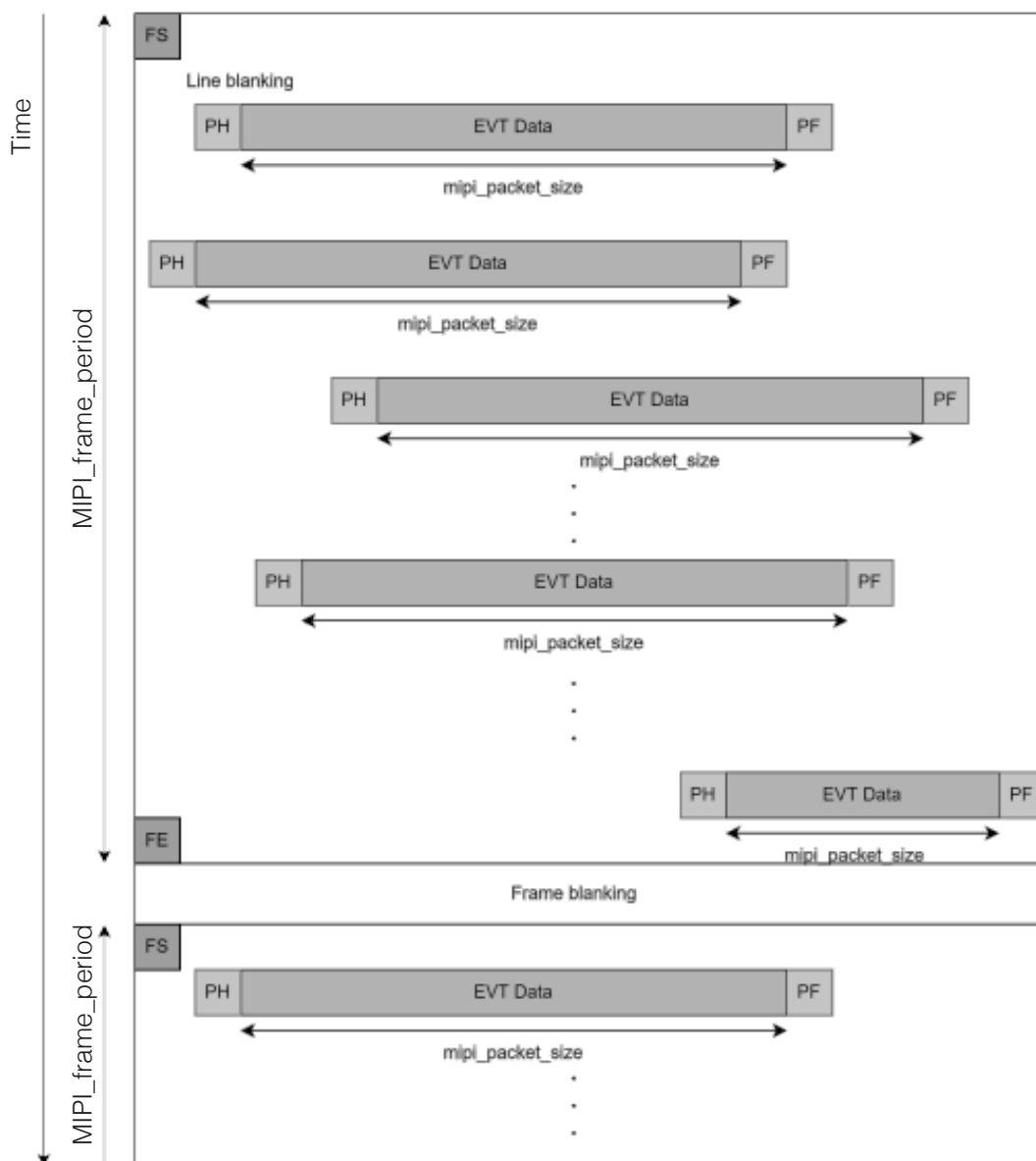


Figure 14. Mechanical drawing: FRAMOS Sensor Module (FSM) of the FSM-IMX636 Devkit

FSM Mechanical Drawing

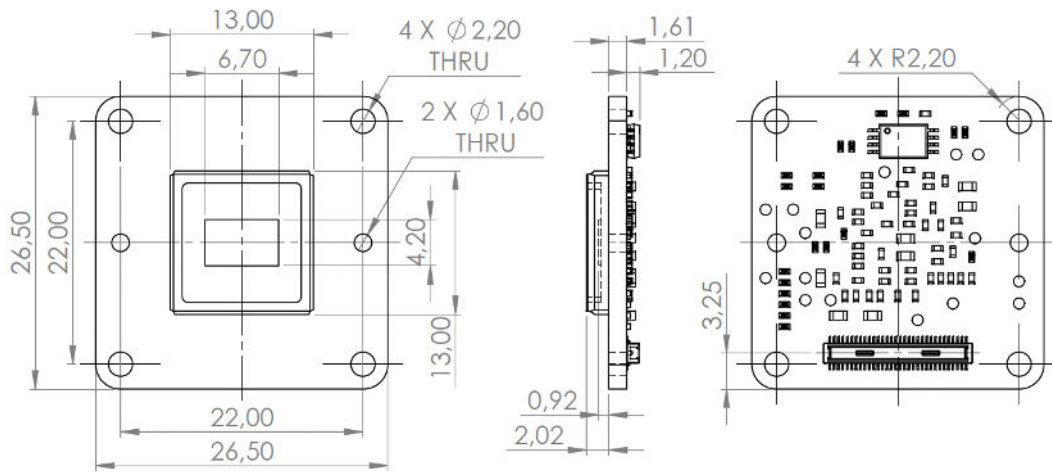


Figure 15. Mechanical drawing: FRAMOS Sensor Module (FSM) of the FSM-IMX636 Devkit

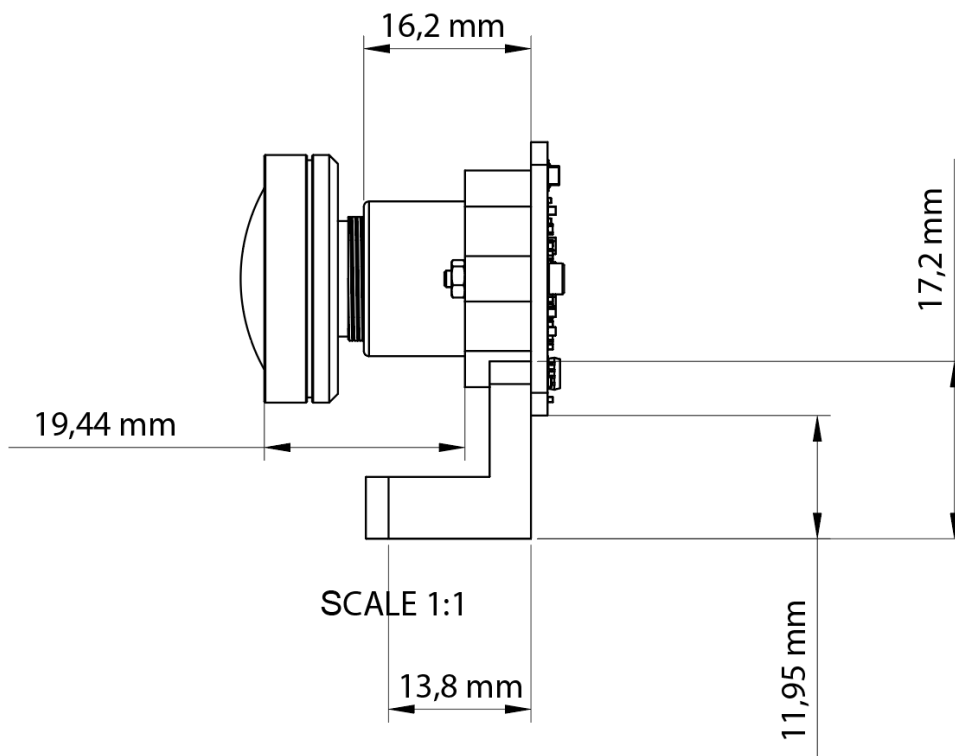


Figure 16. Mechanical drawing: FRAMOS Sensor Module (FSM) of the FSM-IMX636 Devkit

FSM Specifications

For specifications, view the FRAMOS FSM-IMX636 Development Kit Factsheet and Datasheet.

FRAMOS Sensor Adapter (FSA) Overview

The FSA is based on the Crosslink-NX FPGA chip and provides four LDO power supplies with a configurable sequence for the image sensor (3V, 2V5, 1V8, 1V1) and the Crosslink-NX (1V8, 1V).

An onboard oscillator generates a 20 MHz clock, which is connected to the Crosslink-NX. The Crosslink-NX generates the image sensor INCK clock, which is connected to the output PixelMate™ connector. On the output of the PixelMate™ from the FSA, four MIPI data lanes are available (though only two are actively used).

The FSA includes 2x128 Mbit DRAM and 128 Mbit SPI flash for the bitstream. Flashing can be performed through the SPI programming connector or directly to the Crosslink-NX SRAM using JTAG. The current FPGA design for the FSM-IMX636 Devkit does not *actively* use DRAM chips.

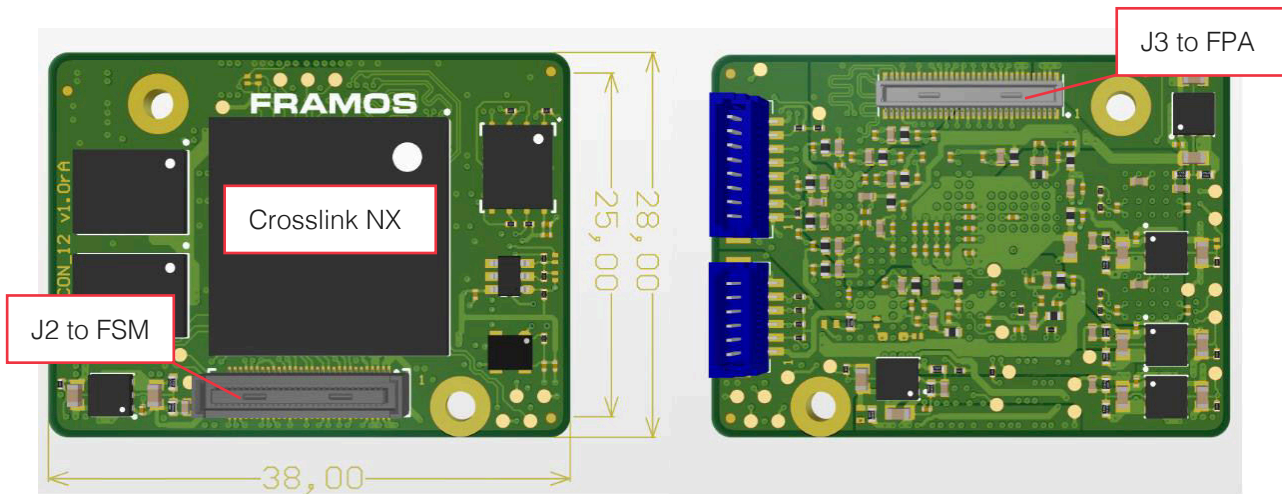


Figure 17. Front and rear view of the design changes to the FSA for FSM-IMX636 Devkit

NOTE The current FPGA design for the FSM-IMX636 Devkit does not actively use the available DRAM chips. The DRAM chips are available for future possible use and can be implemented in your application.

NOTE J3: 60 pin PixelMate™ interconnect interfacing with the FPA. Data exchange routes outwards from here via MIPI TX fixed frame blanking. Data is sent to the processing board for rendering.

FRAMOS Sensor Adapter (FSA) Power Consumption

Power consumption was measured during initial testing with maximum possible events. The results are shown in the table below:

Device Schema Under Test (**Initial Testing)	Power consumption [mW]
FPA-4.A/TXA +FSA-FT27/A-001 + FSM-IMX636E	527,7

FRAMOS Sensor Adapter (FSA) Functionality

The FSA adjusts power supplies, power-up sequence, clock, and control signals for the image sensor to work in application conditions as described in the official Sony sensor datasheet. However, its primary function is to bridge the MIPI CSI-2 to MIPI CSI-2 interface with additional variable frame to fixed frame processing.

The FSA features an internal oscillator that generates a clock, voltage regulators, an 8-pin header connector, a 6-pin header connector, flash memory, two DRAMs, and a Lattice Crosslink-NX FPGA chip. The board includes two groups of voltage regulators, one for generating power supplies for the Crosslink-NX and the other for generating analog, interface, and digital power supplies specified for the specific image sensor. The sequence is controlled within the Crosslink-NX logic.

The FSA relies on the FPA power supplies to generate the necessary power rails, clock, and control signals for the Crosslink-NX and FSM.

To boot the Crosslink-NX from flash memory, the bit file must be flashed to the flash memory via a Lattice Radiant Programmer. Flash programming is available with an external HW programmer through the FSA 8-pin header or over the EE_* pins on a 60-pin PixelMate connector.

The Crosslink-NX can be programmed over the JTAG interface with a Lattice Radiant Programmer. JTAG programming is available with an external HW programmer through the FSA 6-pin header.

FRAMOS Sensor Adapter (FSA) Mechanical Drawing

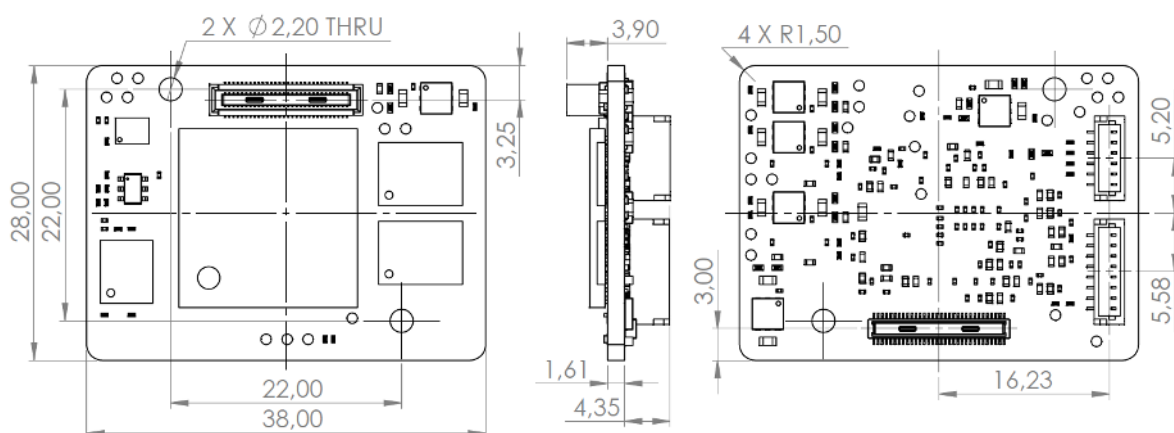


Figure 18. Mechanical drawing: Framos Sensor Adapter (FSA) location in the FSM-IMX636 Devkit

FRAMOS Sensor Adapter (FSA) J3 (PixelMate™ to FPA) Schematic

Reference the below pinouts for your case use:

J3 Pin	Pin Description	J3 Pin	Pin Description
Pin1	3V8_VDD	Pin16	RST_1
Pin2	1V8_VDD	Pin17	EE_MISO
Pin3	3V8_VDD	Pin18	SPI_MISO
Pin4	1V8_VDD	Pin19	XMASTER0
Pin5	NC	Pin20	EE_MOSI
Pin6	NC	Pin21	I2C_0 (SPI_SCK)
Pin7	NC	Pin22	I2C_1_SCL
Pin8	NC	Pin23	SPI_CS
Pin9	NC	Pin24	SYS_PW_EN
Pin10	NC	Pin25	GPIO1(XVS0)
Pin11	GND	Pin26	EE SCK
Pin12	GND	Pin27	I2C (SPI_MOSI)
Pin13	GND	Pin28	I2C_1_SDA
Pin14	GND	Pin29	GPIO2(XHS0)
Pin15	RST_0	Pin30	EE_SS

NOTE Pin 31 to Pin 60 are described in a table on the following page.

FRAMOS Sensor Adapter (FSA) J3 (PixelMate™ to FPA) Schematic (Cont.)

Reference the below pinouts for your case use:

J3 Pin	Pin Description	J3 Pin	Pin Description
Pin31	XTRIG0	Pin46	D_DATA_3_P
Pin32	GPIO11	Pin47	NC
Pin33	PW_EN	Pin48	D_DATA_3_N
Pin34	PROGRAMn	Pin49	GND
Pin35	GPIO6	Pin50	GND
Pin36	GPIO7	Pin51	D_DATA_0_N
Pin37	GND	Pin52	D_DATA_1_N
Pin38	GND	Pin53	D_DATA_0_P
Pin39	MCLK_0	Pin54	D_DATA_1_P
Pin40	MCLK2	Pin55	GND
Pin41	MCLK_1	Pin56	GND
Pin42	MCLK3	Pin57	D_DATA_2_P
Pin43	GND	Pin58	D_CLK_0_P
Pin44	GND	Pin59	D_DATA_2_N
Pin45	NC	Pin60	D_CLK_0_N

NOTE Pin 1 to Pin 30 are described in a table on the previous page.

FRAMOS Sensor Adapter (FSA) Test Points

Reference the below pinouts for your case use:

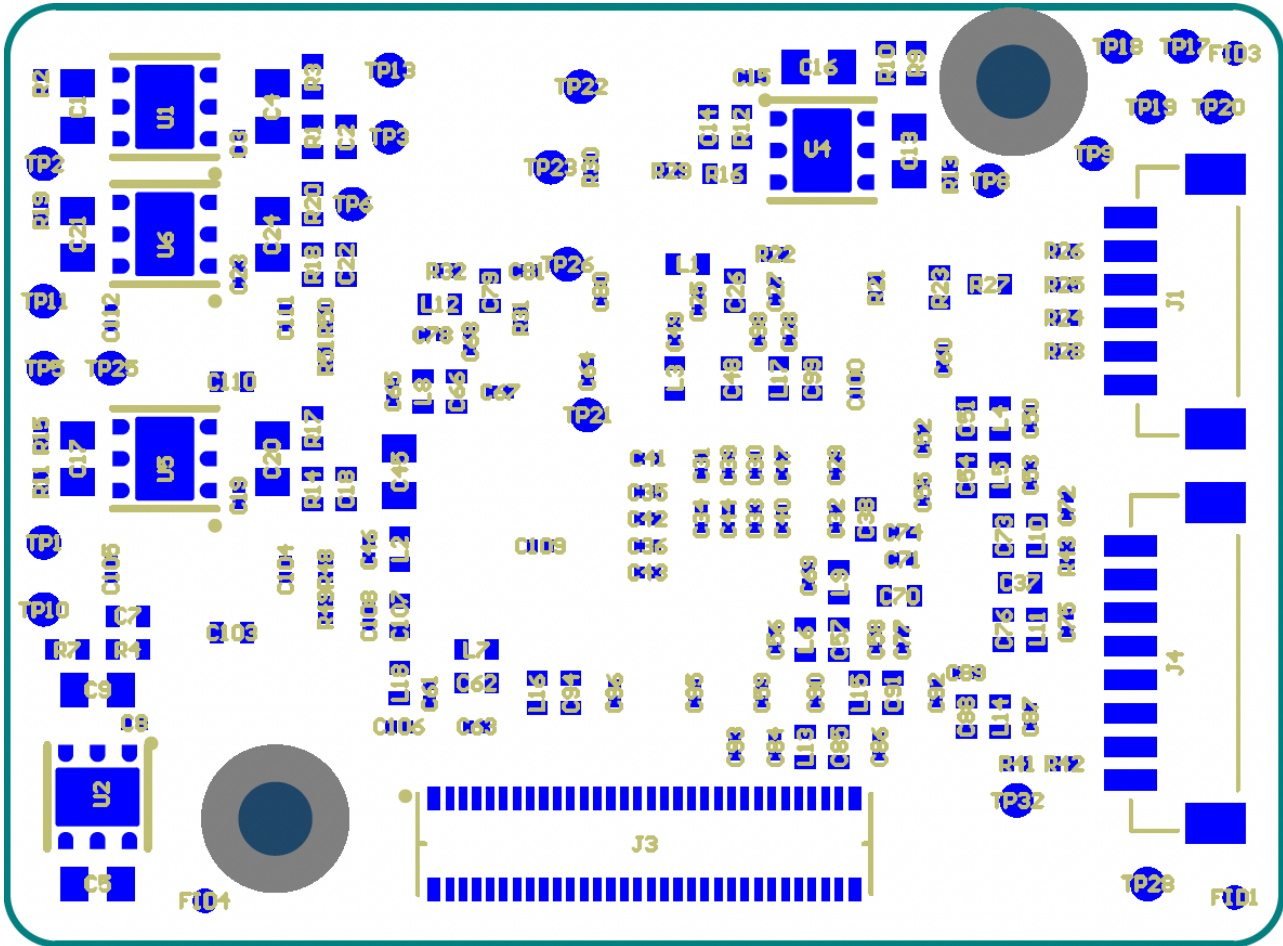


Figure 19. Schematic view of the FSM-IMX636 Devkit FSA rear.

Test Point	Description
TP1	PW EN
TP2	PW EN1
TP3	V_ANA
TP4	GND
TP5	PW EN2
TP6	V_ANA-1
TP7	GND
TP8	PW EN3
TP9	V_DIG
TP10	3V8_VDD

Test Point	Description
TP11	PW EN4
TP12	V_IF
TP13	1V8_VDD
TP14	GP1
TP15	GP2
TP16	GP3
TP17	GP4
TP18	GP5
TP19	GP6
TP20	GND

Test Point	Description
TP21	IS_RST_0
TP22	IS_GPIO1(XVS0)
TP23	IS_MCLK
TP24	IS_GPIO2(XHS0)
TP25	GND
TP26	MCLK_0
TP27	IS_GPIO3(XTRIG)
TP28	GND
TP29	GPIO1(XVS0)
TP30	GPIO2(XHS0)
TP31	GPIO3(XTRIG0)

Connectors: PixelMate™

For more information on the PixelMate™ connector included in this kit, view the [FRAMOS Sensor Module Ecosystem User Manual](#)

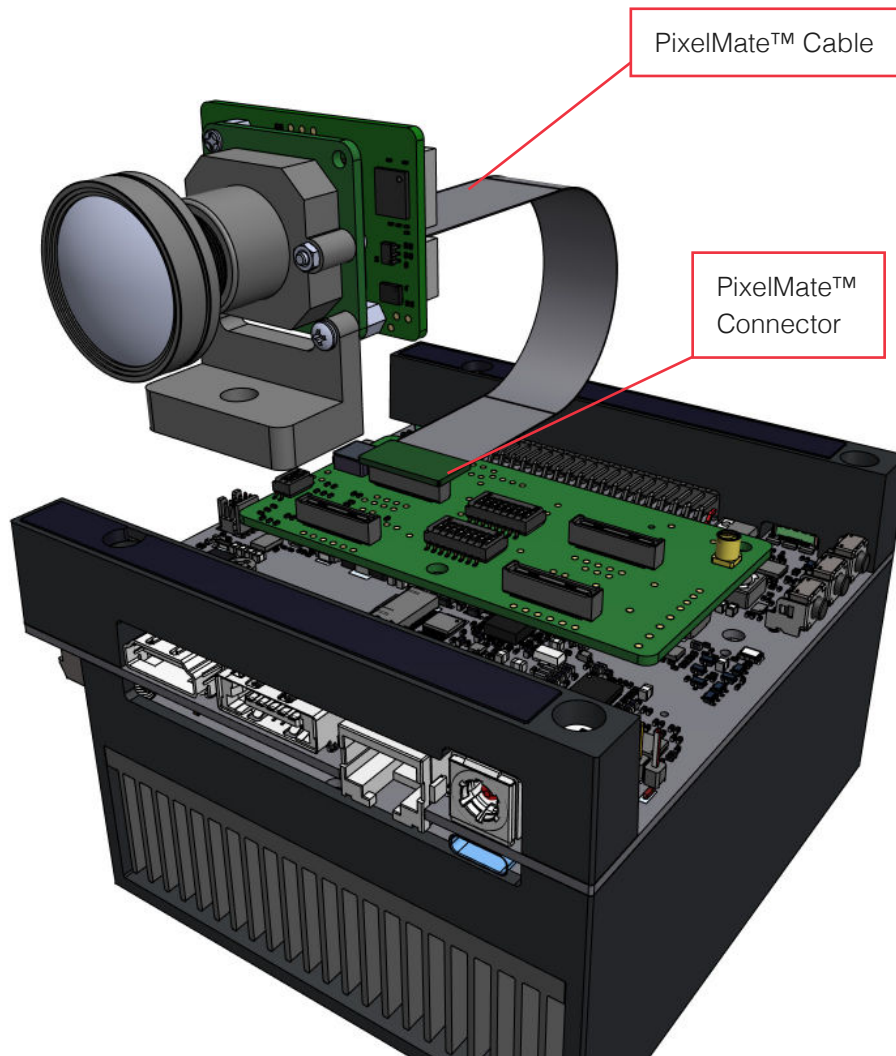


Figure 20. Assembled model view of the FSM-IMX636 Development Kit.

FRAMOS Processor Adapter (FPA)

For more information on the FPA, view the [FRAMOS Sensor Module Ecosystem User Manual](#)

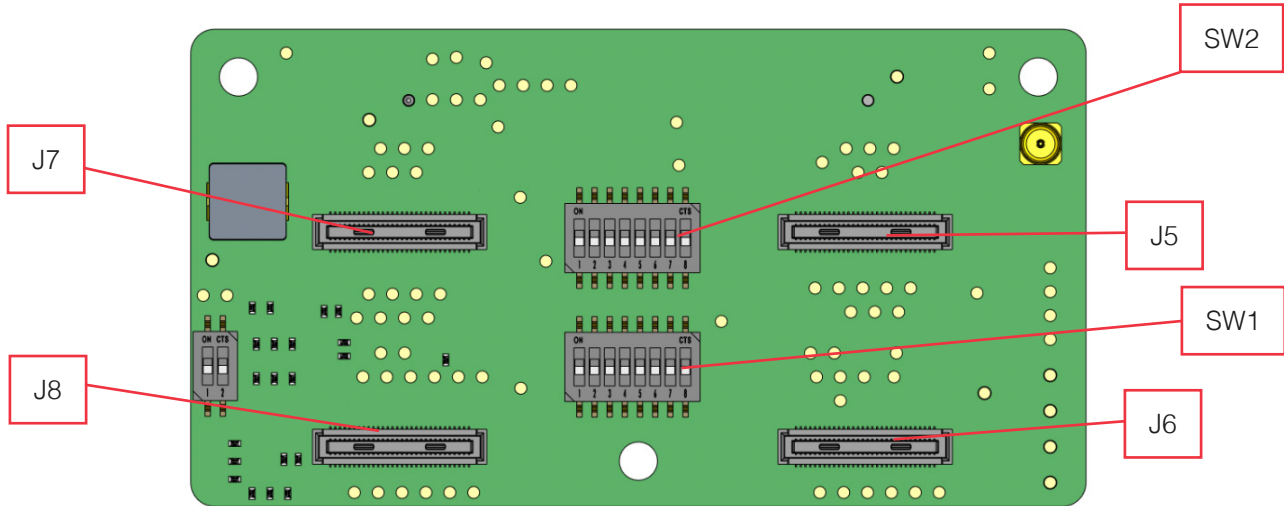


Figure 21. Model view: Front profile of the FRAMOS FPA.

Each of the callouts J7, J8, J5 and J6 are 1 of 4 available Ports on the FPA, each providing 4-Lane CSI-2 that connects to the FSM-IMX636 Devkit through a PixelMate™ connection. Pin 1 must be matched to Pin 1 when connecting.

NOTE SW1 and SW2: Will be described further on the next page.

CAUTION Direct connection of an FSM to the FPA, or wrong cable orientation, will lead to permanent device damage. Using the provided PixelMate™ flex cable (FMA-FC-150/60-v1a) between the FSA and the FPA is mandatory.

FRAMOS Processor Adapter: Multiple Camera Setup (SW1, SW2)

For multiple camera setups, verify the provided FPA (FPA-4.A/TXA-v1a) has the correct DIP switch settings as illustrated below. For more information on the configuration switches, view the [FRAMOS Sensor Module Ecosystem User Manual](#)

NOTE This step is required when running multiple camera setups. For single camera setups, this step can be skipped.

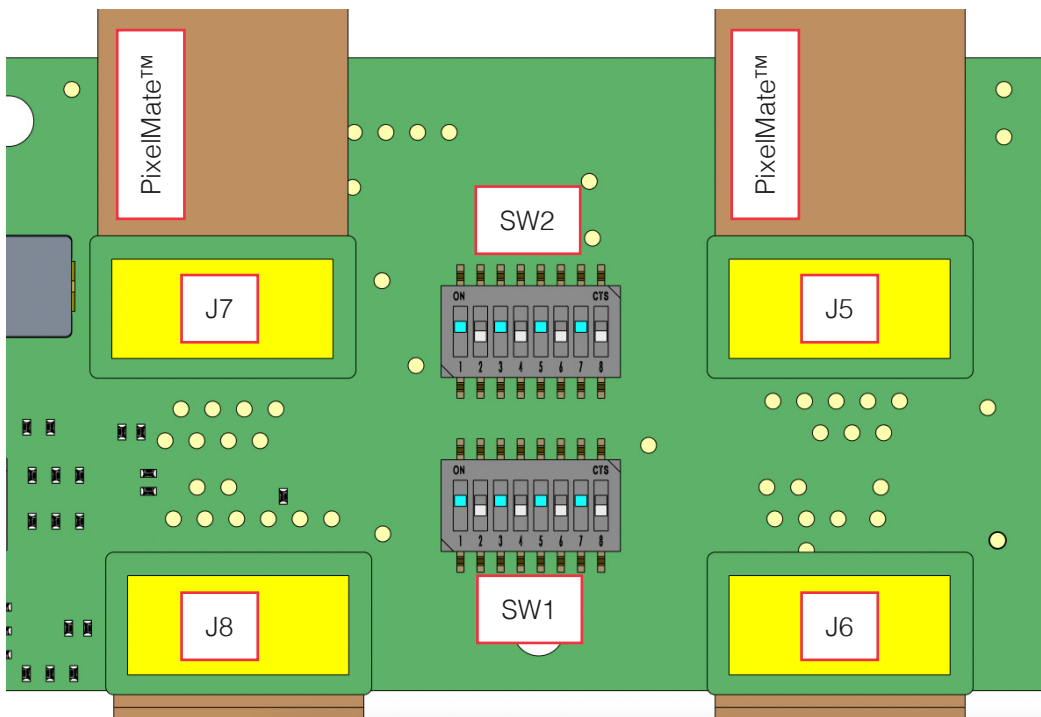


Figure 22. Front view (cut-off) of the correct DIP switch settings on the FPA SW1.

DIP SW	Value (DEFAULT)	Value (Multi-Cam)	Additional Notes
1	0 (OFF)	1 (ON)	Illustrated blue
2	0 (OFF)	0 (OFF)	Illustrated white
3	0 (OFF)	1 (ON)	Illustrated blue
4	0 (OFF)	0 (OFF)	Illustrated white
5	0 (OFF)	1 (ON)	Illustrated blue
6	0 (OFF)	0 (OFF)	Illustrated white
7	0 (OFF)	1 (ON)	Illustrated blue
8	0 (OFF)	0 (OFF)	Illustrated white

FRAMOS Processor Adapter: Multiple Camera Setup (SW1)

DIP switches SW1 and SW2 are mainly for interconnecting FSA triggering signals (XVS, XHS and XTRIG).

DIP switch SW1 is designated to interconnect XVS/XHS pins. If running a multiple camera setup, configure SW1 in accordance with the table values on the previous page. If running a single camera setup, SW1 values can be configured to OFF.

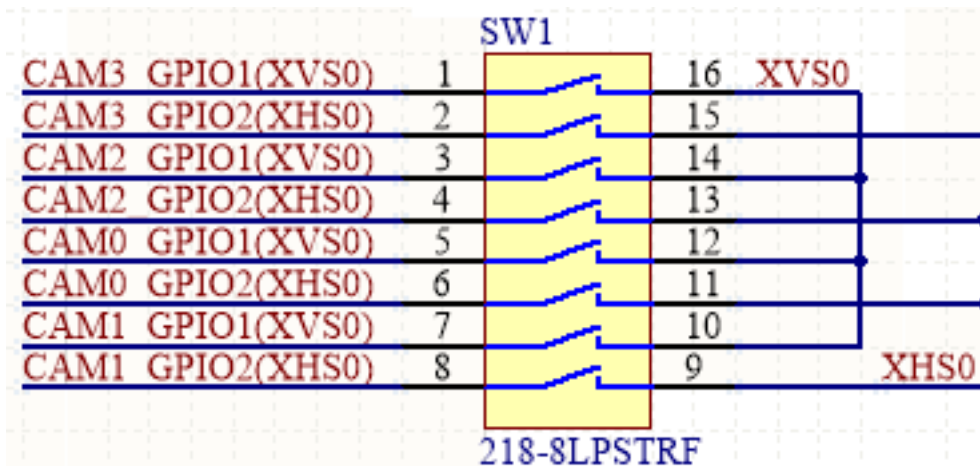


Figure 23. Schematic of FPA SW1.

FRAMOS Processor Adapter: Multiple Camera Setup (SW2)

SW2 is designated to interconnect XTRIG pins and aggregate CAM2_MCLK04(MCLK2) and GPIO25_VDD_SYS_EN(SYS_PW_EN) from the FPA in parallel to all FSA connectors. By default, all positions should be OFF.

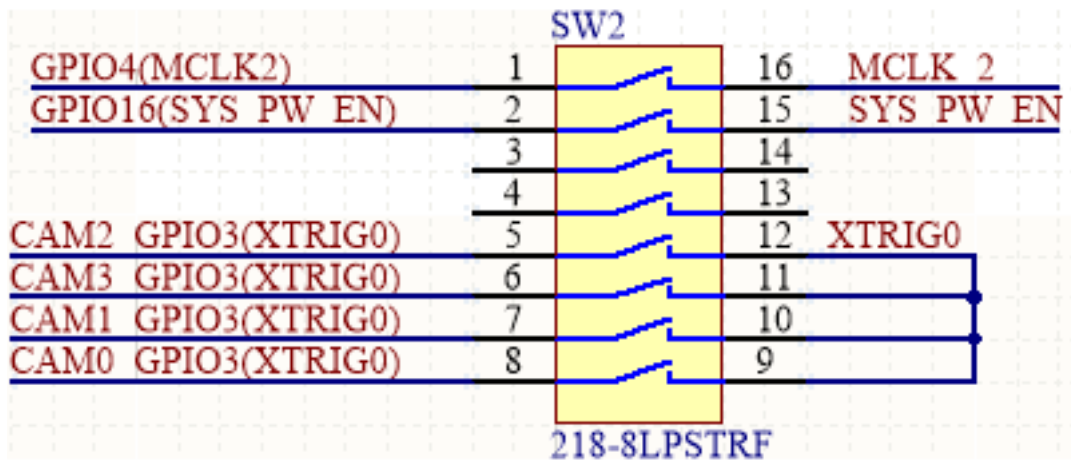


Figure 24. Schematic of FPA SW2.

FRAMOS Processor Adapter: Multiple Camera Setup

This section explains the multi-sensor synchronization function in the event of connecting multiple EVS cameras to the FPA through one of the four available PixelMate™ connectors (J7, J8, J5, or J6). Multi-sensor functionality can be achieved by aligning the intervals of internal timestamp counts, enabling the achievement of the same timestamp values by aligning count start timings.

The external trigger function can be used to create a synchronized system with the external trigger timing as the reference. To operate the multi-sensor synchronization function, use the three functions related to multi-sensor synchronization:

SYNC I/O to Count Interval Synchronization

To achieve consistent internal timestamp count intervals, use the SYNC I/O pin to share the 1 μ s period clock signal for counting timestamps with the host or multiple sensors. If multiple sensors perform count operations using their respective internally generated clocks without sharing the timestamp clock, their operation may be affected by the variance of each clock generation circuit.

This variation can accumulate and result in timestamp deviation, particularly when operated for long durations.

EXTRIG to Count Value Synchronization

Synchronize the internal count values of multiple sensors by simultaneously inputting the trigger signal used for synchronization to the EXTRIG pins.

I2CADDR In. to Allow Sensor Independent Control

Set the registers of sensors connected to the same I2C bus individually by choosing the I2C slave address using the I2CADDR pin.

NOTE Application circuits and system block diagrams are described in the following pages.

CAUTION When using multiple EVS cameras, it is important to set your NVIDIA® processor board to MAXN. Monitoring system temperature for signs of overheating when running multiple EVS cameras.

FRAMOS Processor Adapter: Multiple Camera Setup System Block Diagram (1)

The below diagram illustrates the synchronization schema using EXTTRIG as the trigger signal and the HOST as Master. To implement this, configure all sensors to timestamp count clock slave operation. Apply a 1 microsecond clock from the Host to the SYNC pins to ensure consistent timestamp intervals. Set each sensor to operate as a timestamp count clock slave, then initiate the Host's 1 microsecond clock operation to ensure consistent timestamp values.

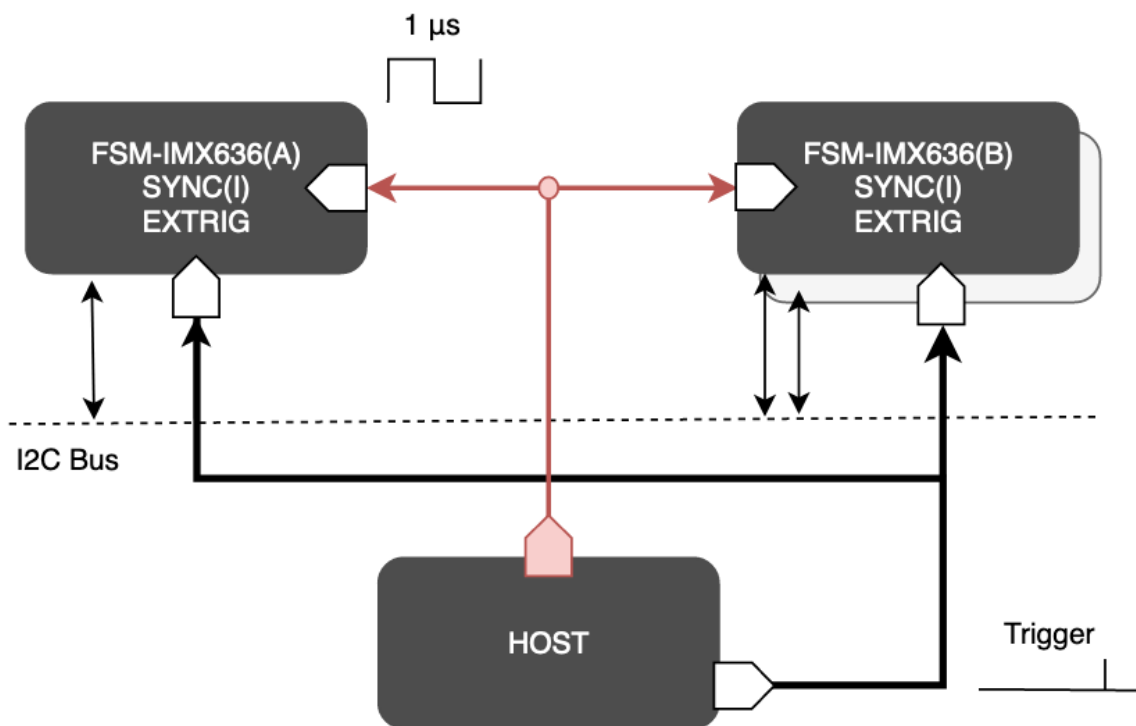


Figure 25. Synchronization setup.

NOTE If the power on/off sensors are mixed, adjust the SYNC terminal input of the power OFF sensor to a low state or a high-impedance state (Hi-Z).

FRAMOS Processor Adapter: Multiple Camera Setup System Block Diagram (2)

To achieve the same with another FSM-IMX636 as Master: configure the IMX636A (or IMX637A) to the master operation standby state. Configure the IMX636B (or IMX637B), and so forth, to slave operation with timestamp count clock.

To achieve the same timestamp count intervals, generate a 1 μ s clock from the SYNC pin of the master IMX636A (or IMX637A) and connect it to the SYNC pins of the slave IMX636B (or IMX637B), and so forth.

Next, configure the slave IMX636B (or IMX637B), and so forth, to timestamp count clock slave operation. Then, set the time_base_enable register of the master IMX636A (or IMX637A) to "1", and initiate the 1 μ s clock operation to ensure the same timestamp values.

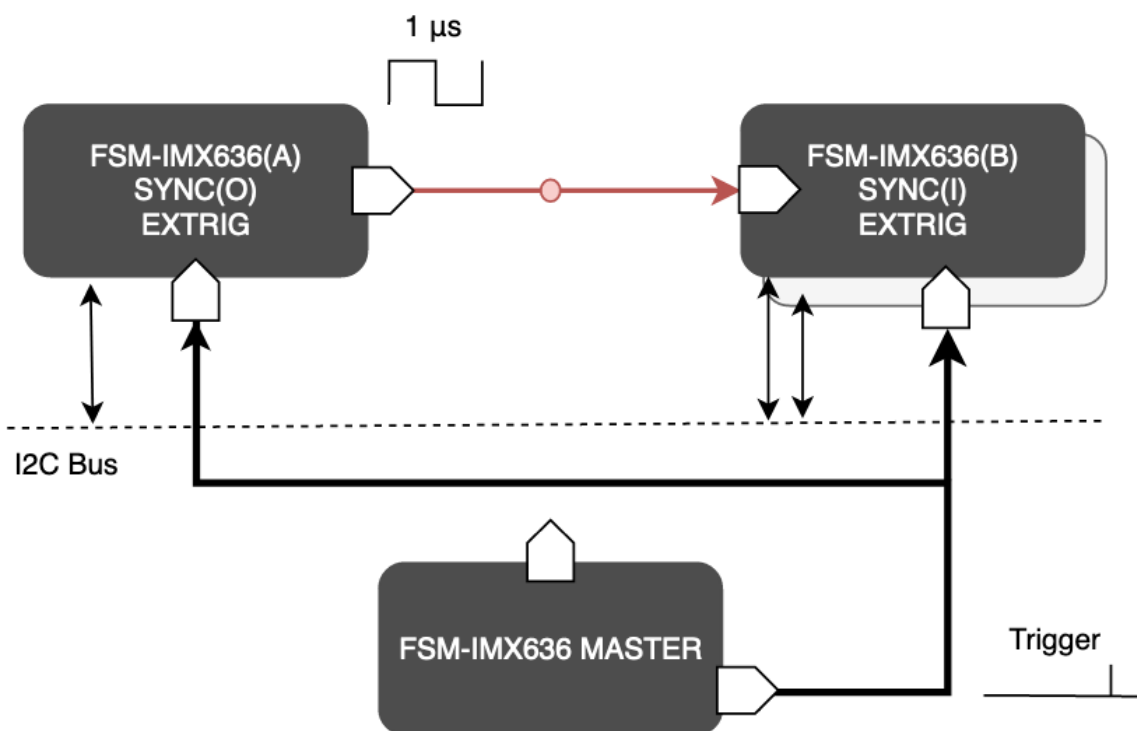


Figure 26. Synchronization setup.

NOTE In case the Master side is ON and the Slave side is OFF, configure the pad_sync register (Address 0x00000044) to 4b'1111 and set the SYNC signal on the Master side to Hi-Z.



SOFTWARE APPENDIX

The following pages elaborate on software controls when configuring environments in advanced use cases.



How the Software Package is Segmented:

This technology was realized in collaboration between Sony® and PROPHESSEE® by combining Sony's CMOS image sensor technology with PROPHESSEE's unique event-based Metavision® sensing technology.

As such, the software is broken into different segments: the *driver* section and the *plugin*. The **driver** section is a standard V4L2 driver with custom V4L2 functions provided by FRAMOS®, and the Metavision® **plugin** is provided by PROPHESSEE® to successfully process events from the IMX636 image sensor.

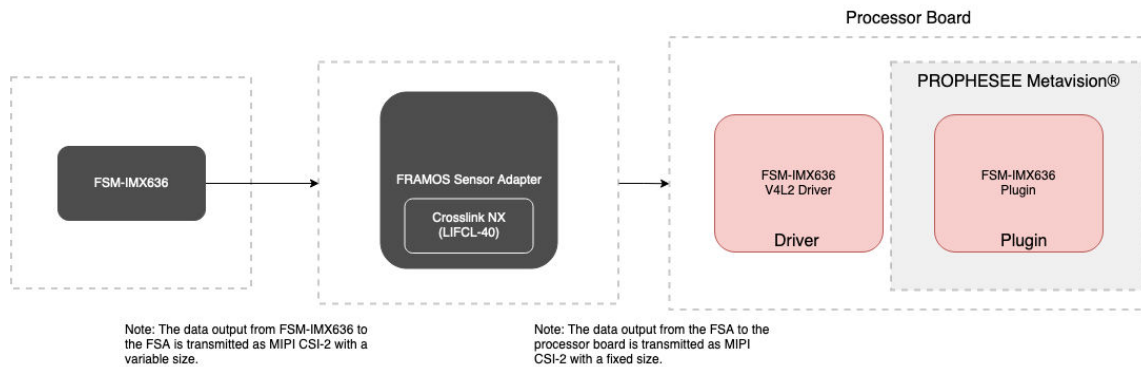


Figure 27. Software segmentation of the FSM-IMX636 Devkit.

The following pages list details about custom controls that were implemented since the FSM-IMX636 is not a traditional frame-based image sensor.

Additional documentation in relation to the Metavision SDK can be found at docs.prophesee.ai

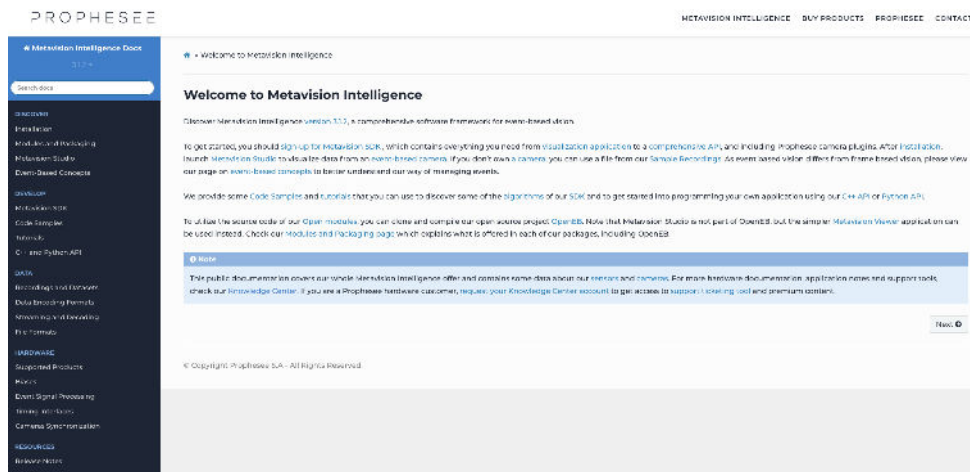


Figure 28. PROPHESSEE® documentation.



IMX636 Driver V4L2 Controls Documentation

Below is information regarding the IMX636 related controls. Though the driver is a standard V4L2 driver, a new FPGA chip is utilized and support for Crosslink-NX was added to the kernel. Since the IMX636 Devkit is not a traditional frame-based image sensor, there are no standard controls such as gain, exposure, and frame rate. Utilize the below custom controls for your specific use cases.

Additional documentation in relation to the Metavision SDK can be found at docs.prophesee.ai

Horizontal Blanking:

This function controls the horizontal blanking display process of the transmitted frame from the Crosslink-NX. Horizontal blanking impacts the time between lines in one frame. Pulse time (or symbol duration time) is noted in this control as unit intervals (UI).

ID	IMX636_CAMERA_CID_CL_HBLANK
Name	Horizontal Blank
Type	Int32
Min	50
Max	0x7FFFFFFF
Step	1
Def	80
Unit	UI

CAUTION When this value is increased from its default settings, the frames per second will decrease and can lead to a Crosslink-NX internal buffer overflow. Increase these settings with caution. **It is not advisable to change this control.**



Vertical Blanking:

This function controls the vertical blanking display process of the transmitted frame from the Crosslink-NX. Vertical blanking impacts the time between lines in one frame. Pulse time (or symbol duration time) is noted in this control as unit intervals (UI).

ID	IMX636_CAMERA_CID_CL_VBLANK
Name	Vertical Blank
Type	Int32
Min	72
Max	0x7FFFFFFF
Step	1
Def	72
Unit	UI

CAUTION When this value is increased from its default settings, the frames per second will decrease and can lead to a Crosslink-NX internal buffer overflow. Increase these settings with caution. **It is not advisable to change this control.**



Changing Latency and BGR with BIAS_FO:

The *BIAS_FO* control is a voltage applied to the reset transistor in a pixel circuit of an image sensor.

The floating diffusion node, which is an output node in the pixel circuit that collects charge generated by the photodiode, is affected by this voltage.

The *BIAS_FO* voltage controls the reset level of the pixel, which determines the sensor's sensitivity. Additionally, the *BIAS_FO* voltage can affect the cutoff frequency of the low-pass filter in the pixel circuit, which impacts the sensor's latency and background rate.

ID	IMX636_CAMERA_CID_BIAS_FO
Name	bias_fo
Type	Int32
Min	45
Max	140
Step	1
Def	48

NOTE There is a tradeoff relationship between the latency and the background rate in machine vision.

Changing Analog Noise Filter Characteristics with BIAS_HPF:

The purpose of this control is to manage analog noise filter characteristics. You can change these by using *BIAS_HPF*. Setting a larger value for the *BIAS_HPF* register value will increase the cutoff frequency inside the analog block, and will reduce the noise level (BGR). It should be noted that doing so will also influence the event generation, relative to the normal brightness changes, particularly on the low illumination side.

ID	IMX636_CAMERA_CID_BIAS_HPF
Name	bias_hbf
Type	Int32
Min	0
Max	120
Step	1
Def	0



Controls for Positive and Negative Thresholds:

The positive and negative thresholds are changed by the below controls; `bias_diff_on`, `bias_diff`, and `bias_diff_off`.

The **reset level** (reference voltage) is changed by `bias_diff`, whereas the **positive threshold** is defined by the difference between `bias_diff_on` and `bias_diff`. The **negative threshold** is defined by the difference between `bias_diff_off` and `bias_diff`.

The positive and negative thresholds represent the voltage change width (brightness change width), starting from the reset level, until a corresponding positive or negative event is generated.

IMX636_CAMERA_CID_BIAS_DIFF_ON

ID	IMX636_CAMERA_CID_BIAS_DIFF_ON
Name	<code>bias_diff_on</code>
Type	Int32
Min	15
Max	255
Step	1
Def	105

IMX636_CAMERA_CID_BIAS_DIFF

ID	IMX636_CAMERA_CID_BIAS_DIFF
Name	<code>bias_diff</code>
Type	Int32
Min	52
Max	100
Step	1
Def	85

WARNING The reference voltage is controlled by `BIAS_DIFF`. **It is not advisable to change this value.**



Controls for Positive and Negative Thresholds (Cont.)

The positive and negative thresholds are changed by the below controls; `bias_diff_on`, `bias_diff`, and `bias_diff_off`.

The **reset level** (reference voltage) is changed by `bias_diff`, whereas the **positive threshold** is defined by the difference between `bias_diff_on` and `bias_diff`. The **negative threshold** is defined by the difference between `bias_diff_off` and `bias_diff`.

The positive and negative thresholds represent the voltage change width (brightness change width), starting from the reset level, until a corresponding positive or negative event is generated.

IMX636_CAMERA_CID_BIAS_DIFF_OFF

ID	IMX636_CAMERA_CID_BIAS_DIFF_OFF
Name	<code>bias_diff_off</code>
Type	Int32
Min	15
Max	255
Step	1
Def	57



Managing 'Dead Time' with BIAS_REFR

Dead time is the duration during which a pixel remains in its reset state after an event has occurred. The pixel cannot generate any events during this time. The value of the bias_refr register can be adjusted to modify the dead time.

Additional information regarding the dead time calculation is seen in the following page.

ID		IMX636_CAMERA_CID_BIAS_REFR
Name	bias_diff_refr	
Type	Int32	
Min	0	
Max	255	
Step	1	
Def	52	

NOTE Increasing the value of the bias_refr register reduces the dead time, but it also decreases the positive event contrast threshold and increases the negative event contrast threshold.

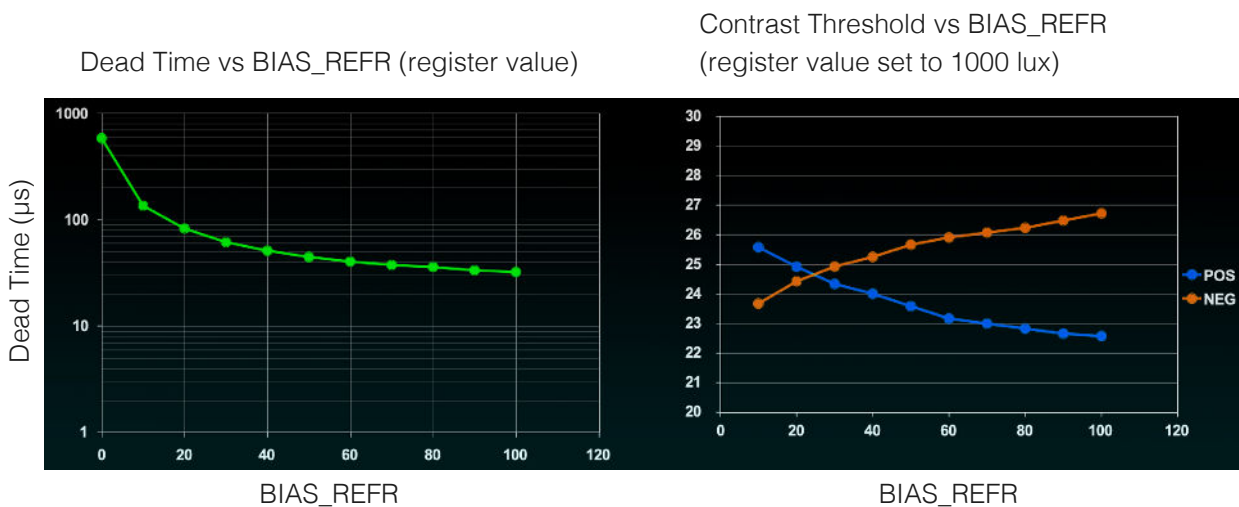


Figure 29. Software dead time illustration with BIAS_REFR.



Calculating 'Dead Time' with BIAS_REFR

The analog block of the sensor includes a test circuit that measures the dead time. This can be achieved by enabling the measurement function.

The circuit counts the time, which is periodically reset based on the value of the bias_refr register. The reset period is set by a clock counter within the digital core, which typically operates at 100 MHz.

By enabling refr_en and refr_cnt_en, refr_counter can be read. The measurement status is indicated by the refr_valid register, where 0 means the measurement is incomplete and 1 means it is complete. Each time the refr_valid register is read, refr_counter is updated.

The diagram below illustrates the flow for measuring dead time using the dead time measurement circuit:

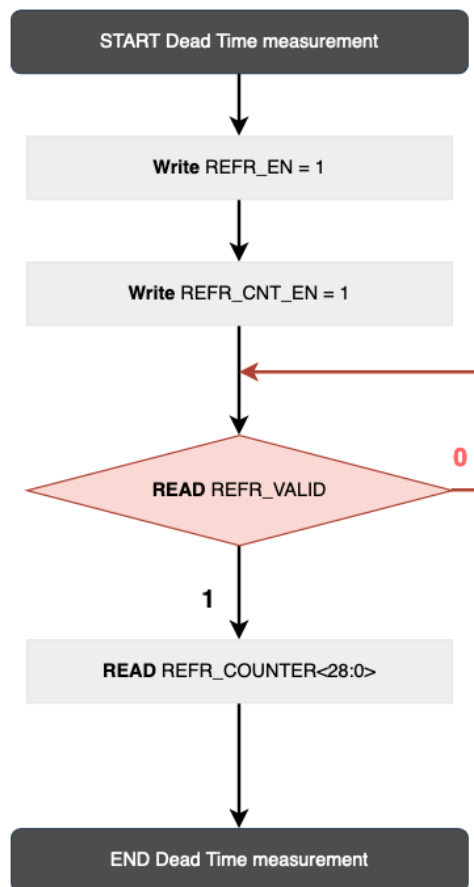


Figure 30. Dead time measurement using BIAS_REFR_EN



Obtain Event Signals from Arbitrary Regions with CID_ANALOG_ROI

This device includes an analog ROI circuit that allows event signals to be obtained from any desired region.

The analog ROI circuit controls pixel circuits by activating or resetting them to capture events. There are two options available for analog ROI region selection: **Analog ROI arbitrary row column specification mode** and **Analog ROI Window mode**.

Additional information regarding the related registers and their field names with bit values can be obtained in the affiliated Sony® IMX636 sensor datasheet.

ID	IMX636_CAMERA_CID_ANALOG_ROI
Name	Analog Roi
Type	UInt32
Min	0
Max	0xFFFFFFFF
Step	1
Def	0
Dims	63

NOTE When transitioning from Analog ROI Window mode to arbitrary row column specification mode, it is necessary to set all the arbitrary row specification registers (roi/td_roi_x00 to x39) and the arbitrary column specification registers (roi/td_roi_y00 to x22).



Set Digital Crop with CID_DIGITAL_CROP

The sensor comes with a digital crop circuit that enables users to specify an arbitrary Crop Window region.

The digital circuit automatically discards any events outside the Crop Window region. Although the Crop Window region can be set independently from the analog ROI region, it's recommended to set them both the same way to avoid losing events.

Additional information regarding the digital crop settings, including Arbitrary Matrix Mode, can be obtained in the affiliated Sony® IMX636 sensor datasheet.

ID	IMX636_CAMERA_CID_DIGITAL_CROP
Name	Digital Crop
Type	UInt32
Min	0
Max	0xFFFFFFFF
Step	1
Def	0
Dims	2

CAUTION The start and end coordinates are subject to the following restrictions:

- They can be changed dynamically.
- In the X direction, the start address must be set to a multiple of 32, and the end address must be set to a multiple of 32-1.
- `dig_crop_end_x` must be greater than `dig_crop_start_x`, and `dig_crop_end_y` must be greater than `dig_crop_start_y`.



Important Software Notices: Analytics Information

Regarding the FRAMOS® IMX636 plugin, it has been implemented with analytics information to address the issue of generating a large number of event packets by the image sensor, particularly in dynamic scenes. Due to the high volume of rich data generated and the significant payload associated with each packet, the processor board may be unable to process the data in a timely manner.

To address this issue, the plugin consists of two threads: the *acquisition thread* and *processing thread*. The **acquisition thread** acquires frames from Crosslink-NX, while the **processing thread** takes a frame from the frame buffer and sends it for decoding to the Metavision® decoder.

Depending on the specific application, decoding and further processing may take a relatively long time. This may result in the acquisition of frames happening faster than their processing, which leads to frames being dropped in order to keep latency between acquisition and processing at a minimum.

As a result, the plugin displays the number of frames acquired, transferred, and dropped in one second, to provide relevant analytics information.

NOTE Metavision®, a software suite by PROPHESSEE®, includes a *hardware abstraction layer*. This **HAL** allows for the processing of event streams generated by event-based cameras. These streams may be prone to data drop or data corruption, which can result in invalid events. To ensure the validity of events, a decoder capable of identifying and discarding corrupted events is essential. The PROPHESSEE® documentation provides detailed information on using the HAL API and configuring violation detections for EVT3 streams. Check out docs.prophesee.ai for more information.



Important Software Notices: Analytics Information

Latency is heavily influenced by the application being used. When displaying a simple image stream, the latency between acquisition and display is typically very low, measured in milliseconds and almost imperceptible to the user. However, for more complex applications, the processing demands may be too high for the platform to handle, rendering the application unusable unless adjustments are made.

In more demanding applications, latency can be noticeable to the human eye, potentially even in seconds, depending on the application.

For this reason, *resource utilization* should be considered.



Important Software Notices: Analytics Information

Resource utilization on the NVIDIA® platforms can vary depending on the scenes being captured. In MAXN mode with 8 cores, still scenes typically use approximately 15% of each core's resources. However, dynamic scenes require more resources, with utilization around 35-40% per core.

NOTE These measurements apply to simple image stream displays.

If running applications on a smaller platform with fewer than 8 cores, resource utilization could be problematic depending on the application's demands. CPU processing may be a bottleneck in such cases. Optimizations such as utilizing GPU cores, CUDA cores, and other platform resources may be possible and could improve processing performance.

It is worth noting that Framos, the source of this information, does not focus on application-level optimizations. The evaluation was conducted using only CPU processing.

NOTE Additional information in how to set your processor board to MAXN mode is available in the FRAMOS® Software User Guide.



CONTACT INFORMATION

Our world-wide talent pool is ready to help ensure your entire product development journey from proof-of-concept to prototyping, and to mass production.

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About FRAMOS | FRAMOS is an imaging expert, trusted advisor, and vision solutions provider. Since 1981, FRAMOS implements the best current and emerging imaging technologies to address specific customer requirements and applications. FRAMOS meets these requirements with advanced and proven imaging components from a global network of renowned partners and with FRAMOS IP.

More than 180 FRAMOS employees world-wide are passionate about the unlimited potential of imaging and help customers achieve the optimum results from every possible scenario. FRAMOS drives and ensures the entire product development journey from POC, through prototyping, to mass production. FRAMOS carefully selects imaging components, like image sensors, lenses, or various 3D technologies, and offers custom developments tailored to individual needs and time frames.

FRAMOS listens to, and understands, customer challenges. With innovative solutions FRAMOS ensures successful project outcomes and develops long-term customer relations.

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