

Ver.1.3

Diagonal 11.0 mm (Type 2 / 3) CMOS solid-state Image Sensor with Square Pixel for Monochrome Cameras

---

## Description

The IMX421LLJ is a diagonal 11.0 mm (Type 2 / 3) CMOS active pixel type solid-state image sensor with a square pixel array and 2.86 M effective pixels. This chip features a global shutter with variable charge-integration time. This chip operates with analog 3.3 V, digital 1.2 V, and interface 1.8 V triple power supply, and has low power consumption. High sensitivity, low dark current and low PLS characteristics are achieved.  
(Applications: FA cameras, ITS cameras)

---

## Features

- ◆ CMOS active pixel type dots
- ◆ Built-in timing adjustment circuit, H/V driver and serial communication circuit
- ◆ Global shutter function
- ◆ Input frequency  
37.125 MHz / 74.25 MHz / 54 MHz
- ◆ Number of recommended recording pixels: 1936 (H) × 1464 (V) approx. 2.83 M pixels
  - Readout mode
  - All-pixel scan mode
  - Vertical / Horizontal 1 / 2 Subsampling mode
  - 2 × 2 Vertical FD binning mode
  - ROI mode
  - Vertical / Horizontal - Normal / Inverted readout mode
- ◆ Readout rate
  - Maximum frame rate in
  - All-pixel scan mode: 8 bit: 409.2 frame/s, 10 bit: 371.8 frame/s, 12 bit: 231.2 frame/s
- ◆ 8-bit / 10-bit / 12-bit A/D converter
- ◆ CDS / PGA function
  - 0 dB to 24 dB: Analog Gain (0.1 dB step)
  - 24.1 dB to 48 dB: Analog Gain: 24 dB + Digital Gain: 0.1 dB to 24 dB (0.1 dB step)
- ◆ I/O interface
  - SLVS (4 ch / 8 ch switching) output (594 / 297 Mbps per ch)
  - SLVS - EC (1 Lane / 2 Lane / 4 Lane / 8 Lane switching) output (2.376 / 1.188 Gbps per Lane)
- ◆ Recommended lens F number: 2.8 or more (Close side)
- ◆ Recommended exit pupil distance: -100 mm to  $-\infty$

## Pregius

\* Pregius is a registered trademark or trademark of Sony Group Corporation or its affiliates. The Pregius is global shutter pixel technology for active pixel-type CMOS image sensors that use Sony's low-noise CCD structure, and realizes high picture quality.

Sony reserves the right to change products and specifications without prior notice.

"Sony", "SONY" logo are registered trademarks or trademarks of Sony Group Corporation or its affiliates.

**Device Structure**

◆ CMOS image sensor			
◆ Image size	Diagonal 11.0 mm (Type 2 / 3)	Approx. 2.86 M pixels	All-pixel
◆ Total number of pixels	1944 (H) × 1496 (V)	Approx. 2.90 M pixels	
◆ Number of effective pixels	1944 (H) × 1472 (V)	Approx. 2.86 M pixels	
◆ Number of active pixels	1944 (H) × 1472 (V)	Approx. 2.86 M pixels	
◆ Number of recommended recording pixels	1936 (H) × 1464 (V)	Approx. 2.83 M pixels	All-pixel
◆ Unit cell size	4.5 μm (H) × 4.5 μm (V)		
◆ Optical black	Horizontal (H) direction: Front 0 pixel, rear 0 pixel Vertical (V) direction: Front 24 pixels, rear 0 pixel		
◆ Package	226 pin LGA		

**Image Sensor Characteristics**

(Tj = 60 °C)

Item		Value	Remarks
Sensitivity (F8)	Typ.	1677 mV	1/30 s accumulation
Saturation signal	Min.	1001 mV	

**Basic Drive Mode**

Drive mode	Recommended number of recording pixels	Maximum frame rate [frame/s]	Output interface	ADC [bit]
All pixel	1936 (H) × 1464 (V) approx. 2.83 M pixels	174.6	SLVS 8 ch	8
		409.2	SLVS – EC 8 Lane	
		143.0	SLVS 8 ch	10
		371.8	SLVS – EC 8 Lane	
		121.1	SLVS 8 ch	12
		231.2	SLVS – EC 8 Lane	
Vertical / Horizontal 1/2 subsampling	968 (H) × 732 (V) approx. 0.71 M pixels	596.7	SLVS 8 ch	8
		780.5	SLVS – EC 8 Lane	
		498.9	SLVS 8 ch	10
		710.8	SLVS – EC 8 Lane	
		425.7	SLVS 8 ch	12
		446.2	SLVS – EC 8 Lane	
2 × 2 Vertical FD binning	968 (H) × 732 (V) approx. 0.71 M pixels	599.6	SLVS 8 ch	8
		784.4	SLVS – EC 8 Lane	
		501.5	SLVS 8 ch	10
		714.3	SLVS – EC 8 Lane	
		427.8	SLVS 8 ch	12
		448.4	SLVS – EC 8 Lane	

