SONY

Tentative Ver.0.1

IMX925-AMJ

Diagonal 19.3 mm (Type 1.2) CMOS solid-state Image Sensor with Square Pixel for Monochrome Cameras

Description

The IMX925-AMJ is a diagonal 19.3 mm (Type 1.2) CMOS active pixel type solid-state image sensor with a square pixel array and 24.55 M effective pixels. This chip features a global shutter with variable charge-integration time. This sensor operates with 3.3 V, 2.9 V, 1.1 V, and 1.8 V quadruple power supply. High sensitivity and low dark current characteristics are achieved.
(Applications: FA cameras, 3D vision cameras)

Features

- ◆CMOS active pixel type dots
- ◆Built-in timing adjustment circuit, H/V driver and serial communication circuit
- ◆Global shutter function
- ◆Input clock frequency 37.125 MHz / 74.25 MHz
- ◆Number of recommended recording pixels: 5320 (H) × 4600 (V) approx. 24.47 M pixels
- ◆Readout mode
  - All-pixel scan mode
  - 1/2 subsampling mode
  - H2V2 FD binning mode / H1V2 FD binning mode / H2V1 FD binning mode
  - ROI mode
  - Vertical / Horizontal - Normal / Inverted readout mode
- ◆Readout rate
  - Maximum frame rate in All-pixel scan mode: *controller mode
  - 8-bit 442.7 frames/s,10-bit 394.2 frame/s, 12-bit 212.6 frame/s (T.B.D)
  - (*) At high frame rates, control so as not to exceed Tj = +100 °C
- ◆Variable-shutter speed
- ◆Pulse Output Function
  - The monitor output for Integration period (TOUT0)
  - The monitor output for internal AD period (TOUT1)
- ◆8-bit / 10-bit / 12-bit A/D converter (Full range)
- ◆CDS / PGC function
  - 0 dB to 24 dB: Variable analog Gain (0.3 dB step)* 12-bit
  - 24.1 dB to 48 dB: Fixed analog Gain: 24 dB + variable digital Gain: 0.3 dB to 24 dB (0.3 dB step)*12-bit
  - 0 dB to 18 dB: Variable analog Gain (0.3 dB step)* 8-bit / 10-bit
  - 18.1 dB to 42 dB: Fixed analog Gain: 18 dB + variable digital Gain: 0.3 dB to 24 dB (0.3 dB step)*8-bit / 10-bit
- ◆I/O interface
  - SLVS-EC (1 Lane , 2 Lane , 4 Lane , 6 Lane , 8 Lane , 4 Lane × 2 , 6 Lane × 2 , 8 Lane × 2) output
  - SLVS-EC Baud Rate: 4.752Gbps / lane 9.504Gbps / lane 12.474Gbps / lane (Grade 3, 4 and 5)

Pregius S

* Pregius S and its logo are registered trademarks or trademarks of Sony Group Corporation or its affiliates. Pregius S is a global shutter sensor technology for active pixel-type CMOS image sensors. By stacking the signal processing on the back illuminated type CMOS Image Sensor it realizes small chip size and high sensitivity, whilst using the high picture quality global shutter pixel technology of Pregius.

Device Structure

◆CMOS image sensor		
◆Image size	Diagonal 19.3 mm (Type 1.2)	Approx. 24.55 M pixel
◆Total number of pixels	5328 (H) × 4672 (V)	Approx. 24.89 M pixel
◆Number of effective pixels	5328 (H) × 4608 (V)	Approx. 24.55 M pixels
◆Number of active pixels	5328 (H) × 4608 (V)	Approx. 24.55 M pixel
◆Number of recommended recording pixels	5320 (H) × 4600 (V)	Approx. 24.47 M pixels
◆Unit cell size	2.74 µm (H) × 2.74 µm (V)	
◆Optical black	Horizontal (H) direction: Front 0 pixels, rear 0 pixel Vertical (V) direction: Front 64 pixels, rear 0 pixel	
◆Package	318 pin LGA	24.5 mm (H) × 21.4 mm (V)

Image Sensor Characteristics

(Tj = 60 °C)

Item		Value	Remarks
Sensitivity	Typ.	TBD Digit/lx/s	
Saturation signal	Min.	TBD Digit	

Basic Drive Mode

Drive mode	Recommended number of recording pixels	Maximum frame rate [frame/s]	Output interface	ADC [bit]
All pixel	5320 (H) × 4600 (V) Approx. 24.47 M pixels	442.7	SLVS-EC 8 × 2 Lane	8
		394.2		10
		212.6		12

Note: All of frame rate are tentative.

Image Sensors for Industrial Applications:
https://www.sony.net/cis-industry